Jetson AGX Orin Series Pin and Function Names Guide

Application Note

DA-11060-001_v1.0 | August 2022

Document History

DA-11060-001_v1.0

Version	Date	Description of Change
1.0	August 8, 2022	Initial release

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Introduction

The NVIDIA® Jetson AGX Orin™ series System on Module (SOM) is built around the NVIDIA Orin™ System on Chip (SoC). Jetson AGX Orin series documentation often refers to names of interfaces, pins, functions, and so on, from a SOM perspective. However, other documentation (for example, the TRM) will necessarily take an SoC perspective. Some documentation will reference both SOM and SoC naming. It is important to understand whether a given document is using the following with reference to the SOM or the SoC.

- Pin names and numbers
- Interface names and instances
- Function names and instances

Note: References to Jetson AGX Orin apply to any of the Jetson AGX Orin series of modules.

Various documents are provided to help customers design, lay out, build, and configure NVIDIA® Jetson™ module-based designs.

Table 1 lists the main documents that are focused on the hardware or contain references to hardware features.

Table 1. Hardware References and Feature Documentation

Document Category	Document Name for Jetson AGX Orin Designs	Description
Data sheet	Jetson AGX Orin Series Module Data Sheet	• Module overview • Power and system management • Interface and signal description • Electrical, package, and thermal specifications
Technical Reference Manual (TRM)	Orin (SoC) Technical Reference Manual	• Address map • Chapters per block (functional description, programming guidelines, and registers)
Product design guide	Jetson AGX Orin Series Design Guide	• Power • Interface chapters (connection figures and tables, and routing guidelines)

Document Category	Document Name for Jetson AGX Orin Designs	Description
Carrier board specification	Jetson AGX Orin Developer Kit Carrier Board Specification	• Developer Kit features and description • Expansion connector and interface descriptions • Power allocation
Pin mux	Jetson AGX Orin Series Module Pin mux	• Module pin name and number, SoC ball name, Verilog ball name. • SFIO and GPIO options • Wakes, straps POR state
Design files	Jetson AGX Orin Developer Kit Carrier Board Design Files	• Schematics, layout, bill of materials (BOM) • Miscellaneous (Assy drawing, stack-up, gerbers, and so on)

Pin and Function Names

There are different pin and interface names in many cases on the module compared to chip. Some documents are based on the chip, such as the TRM, while others are based on the module, or may have both chip and module terms and names. This can lead to confusion. It is important to use the right document and to understand whether a term or name is associated with a chip, module pin name or number, an interface name or instance, or a function name or instance. Table 2 shows what name forms are used in the various documents.

Table 2. Pin Name Usage

Usage	Verilog Name	SoC Ball Name	Module Pin Name
Usage in Documents	Pin mux TRM	Pin mux Design guide	Pin mux Data sheet Design guide Reference design

Pin Mux

The Jetson AGX Orin module pin multiplexing (pin mux) spread sheet has the module pin names and pin numbers in the first two columns. The SoC Verilog and package ball names are in the 3rd and 4th columns. The GPIOs and SFIO functions are covered in the pin muxing area. The portion of the pin mux in Table 3 includes one of the I2S interfaces.

Table 3. Pin Mux I2S and MCLK

Jetson AGX Orin CVM Connector		Verilog Ball Name	Package Ball Name	Pad info	POR	Function
Pin #	Signal Name			Pull Strength	Pin State	Customer Usage
L14	I2S1_CLK	SOC_GPIO45	GP169	50k	pd	I2S1_SCLK
C7	I2S1_SDOUT	SOC_GPIO46	GP170	50k	pd	I2S1_SDATA_OUT
H8	I2S1_SDIN	SOC_GPIO47	GP171	50k	pd	I2S1_SDATA_IN
D8	I2S1_FS	SOC_GPIO48	GP172	50k	pd	I2S1_LRCK
H9	MCLK01	SOC_GPIO59	GP167	50k	pd	AUD_MCLK

In the case shown in Table 3, for one of the I2S interfaces that are available on the module pins, the following pin and function names exist:

- Module signal names: I2S1_xxx
- Verilog ball names: SOC_GPIOxx
- Package (SoC) ball names: GPxxx
- Customer Usage (w/I2S1 pins functions selected): I2S1_xxx

This shows that the module pin names, chip Verilog ball names, chip ball names, and function names can be different. When referring to the various documents, it is important to understand which name form is applicable. For instance, if the TRM is accessed for information on how to configure the pins or functions, it is necessary to know that the TRM is chip focused. It will have SoC Verilog ball names when referring to the pins, such as in the "Pin Mux Register" section, or function names (Customer Usage column of Pin Mux) if the function is being configured. In the case of the module data sheet, the module pin names are relevant. See the following "Data Sheet" and "Technical Reference Manual" sections for details.

Data Sheet

The module data sheet only uses the module pin names. If a programmer needed to know what SoC function to configure, it would be necessary to look at either the pin mux spread sheet or OEM product design guide to know what SoC function is associated with that module pin.

Table 4. Data Sheet I2S1 and MCLK Pin Descriptions

Pin #	Signal	Usage and Description	Direction	Pin Type	Power-on Reset Default
C7	I2S1_SDOUT	I2S Audio Port 1 Data Out	Bidir	CMOS – 1.8V	pd
D8	I2S1_FS	I2S Audio Port 1 Left/Right Clock	Bidir	CMOS – 1.8V	pd
H8	I2S1_SDIN	I2S Audio Port 1 Data In	Bidir	CMOS – 1.8V	pd
L14	I2S1_CLK	I2S Audio Port 1 Clock	Bidir	CMOS – 1.8V	pd
H9	MCLK01	Audio Codec Initiator Clock or GPIO #44	Bidir	CMOS – 1.8V	pd

Note: The pin directions in the data sheet indicate bidirectional since the pins support both SFIO and GPIO functionality. The same pins in the design guide (see Table 5) have Input or Output for some of the pins since the SFIO function is assumed. There are notes under the design guide pin description tables describing the difference in direction between whether the pins are used for SFIOs or GPIOs.

Technical Reference Manual

The technical reference manual (TRM) is based on the chip (for example, SoC Orin). References to pin names (such as SOC_GPIO45) will be Verilog ball names. The TRM also has references to functions (such as I2S1). These should match the names of functions in the pin mux spreadsheet or design guide. To know what pin on the module an SoC pin is associated with, the pin mux spreadsheet is the best cross reference since it includes the module, SoC Verilog, and SoC package ball names.

The following example shows a portion of the pad control for the module I2S1_CLK (Verilog ball name SOC_GPIO45).

PADCTL_G7_SOC_GPIO45_0
Offset: 0x0
Read/Write: R/W
Parity Protection: Y
Shadow: N
SCR Protection: PADCTL_G7_SCR_SCR_SOC_GPIO45_0
Reset: 0x00000414 (0bxxxx,xxxx,xxxx,xxxx,xxx0,x1x0,00x1,0100)

1:0	RSVD0	**PM**: **0** = RSVD0 **1** = I2S1 **2** = RSVD2 **3** = RSVD3

Design Guide

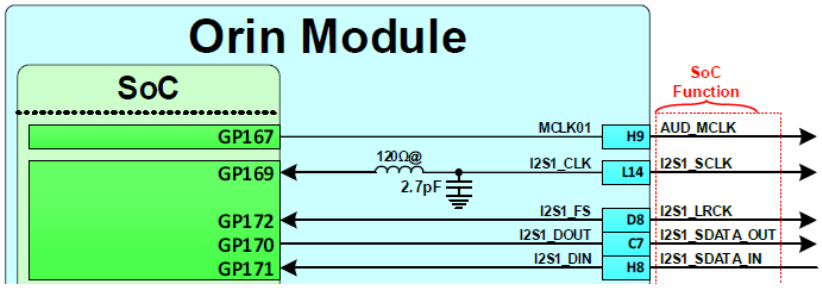
The design guide focuses on the module, but many of the figures and pin description tables also include the SoC signal (package ball name) associated with a module pin where applicable. The partial table (Table 4) contains the same I2S interface used as the example in the earlier sections. Both the module (Jetson AGX Orin) and SoC pin names are shown.

Table 5. Design Guide Audio I2S and MCLK Pin Descriptions

Pin #	Module Pin Name [SoC Audio Function]	SoC Signal	Usage and Description	Direction	Pin Type
H9	MCLK01	GP167	Audio Codec Master Clock	Output	CMOS – 1.8V
L14	I2S1_CLK	GP169	I2S Audio Port 1 Clock	Bidir	CMOS – 1.8V
D8	I2S1_FS	GP172	I2S Audio Port 1 Left/Right Clock	Bidir	
C7	I2S1_SDOUT	GP170	I2S Audio Port 1 Data Out	Output	
H8	I2S1_SDIN	GP171	I2S Audio Port 1 Data In	Input	

Figure 1 also shows the I2S interface and includes the chip and module pin names. In addition, the reference schematic net names are used outside the module. The net names may match the form used for the chip pin names, as in the following example, but not in all cases.

Figure 1. I2S1 Interface



The following AU connections table contains only the module pin names, or function names in parentheses, if necessary, for clarity.

Table 6. Design Guide Audio I2S and MCLK Signal Connections

Module Pin Name (SoC Function)	Type	Termination	Description
I2Sx_CLK (I2Sx_CLK)	I/O	120Ω Bead in series and 2.7 pF capacitor to GND (on Orin module).	I2S Serial Clock: **Connect to I2S/PCM** CLK **pin of AU device.**
I2Sx_FS (I2Sx_LRCK)	I/O		I2S Left/Right Clock: **Connect to Left/Right Clock pin of AU device.**
I2Sx_DOUT (I2Sx_SDOUT)	I/O		I2S Data Output: **Connect to Data Input pin of AU device.**
I2Sx_DIN (I2Sx_SDIN)	I		I2S Data Input: **Connect to Data Output pin of AU device.**
AUD_MCLK	O		Audio Codec Master Clock: **Connect to clock pin of Audio Codec.**

Developer Kit Carrier Board Specification

The developer kit specification uses module (Jetson AGX Orin) pin names and net names from the carrier board reference design. If it is necessary to know the corresponding SoC name or function, the pin mux should be referenced (the design guide also contains similar information except for the Verilog ball names, which are used in the TRM).

Figure 2. I2S and MCLK Connections to Audio Codec

Table 2-15. Audio Panel Header Pin Description

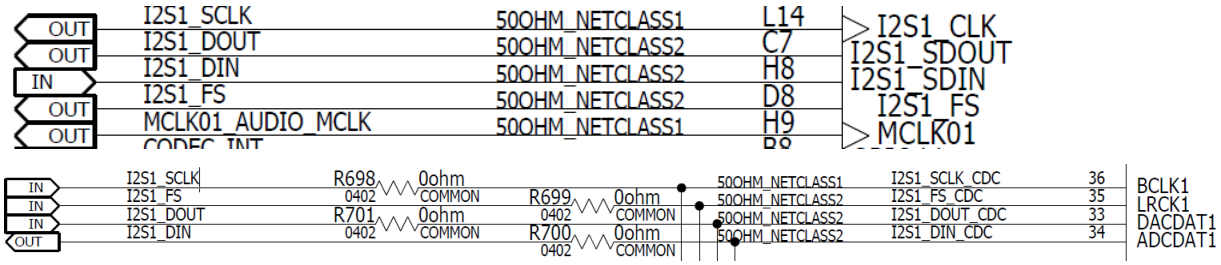
Pin #	Connector (Codec) Pin Name	Associated Module Pin Name	Module Pin #	Usage/Description	Type/Dir
1	(IN1P)	–	–	Microphone #1 input	Input
2	AGND	–	–	Ground	GND
3	(IN2P)	–	–	Microphone #2 input	Input
4	(LRCK2/GPIO4/PDM_SDA)	–	–	Presence – detects if audio dongle is connected to header.	Input
5	(HPO_R)	–	–	Headphone output right channel	Output
6	(MIC_IN_DET)	–	–	Jack/Microphone detect pin	Input
7	SENSE_SEND	–	–	Pulled to analog GND	NA
8	Key				
9	(HPO_L)	–	–	Headphone output left channel	Output
10	(BCLK2/GPIO3/PDM_SCL)	–	–	Headphone or jack detection	Input
–	–	AUDIO_MCLK	H9	Audio master clock	Output
–	–	I2S1_CLK	L14	I2S #1 clock	Output
–	–	I2S1_FS	D8	I2S #1 field select	Bidir
–	–	I2S1_SDOUT	C7	I2S #1 data output	Output
–	–	I2S1_SDIN	H8	I2S #1 data input	Input
–	–	GPIO11	B8	Audio interrupt	Output
–	–	I2C5_CLK	A53	I2C #5 clock	Bidir
–	–	I2C5_DAT	C53	I2C #5 data	Bidir

Notes: In the Type/Dir column, Output is to Audio Header. Input is from Audio Header. Bidir is for bidirectional signals.

Reference Design Files

The reference design files (schematics, layout, and so on) also contain only module pin names and net names. Look to the pin mux or OEM design guide if it is necessary to know which chip pin is associated with a module pin name.

Figure 3. Design Schematics



Chip, Module, and Carrier Board Pin Name and Numbers

The information provided in the following table can be found in various hardware documentation (as described within this application note). Table 7 provides a consolidation of this information for your convenience.

Table 7. Chip, Module, and Carrier Board Pinout

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
A3	PRSNT0	Tied to GND	–
A4	SDCARD_D2	SDMMC1_D2	GP133_SDMMC_A2
A5	SDCARD_CMD	SDMMC1_CMD	GP130_SDMMC_A_CMD
A6	UFS0_REF_CLK	UFS0_REF_CLK	GP173_UFS_A_REFCLK
A7	GPIO29	CAM_ERROR3	GP165
A8	PEX_WAKE_N	PCIE_WAKE_N	GP185_PCIE_WAKE_N
A9	GND	GND	–
A10	USB2_P	USB2_2_P	HS_USB0_P2_P
A11	USB2_N	USB2_2_N	HS_USB0_P2_N
A12	GND	GND	–
A13	GND	GND	–
A14	UPHY_RX8_N	UPHY_RX8_N	HS_UPHY2_L6_RX_N
A15	UPHY_RX8_P	UPHY_RX8_P	HS_UPHY2_L6_RX_P
A16	GND	GND	–
A17	GND	GND	–
A18	UPHY_RX4_P	SNN_UPHY_RX4_P	HS_UPHY2_L2_RX_P
A19	UPHY_RX4_N	SNN_UPHY_RX4_N	HS_UPHY2_L2_RX_N
A20	GND	GND	–
A21	GND	GND	–
A22	UPHY_RX0_P	UPHY_RX0_P	HS_UPHY0_L0_RX_P
A23	UPHY_RX0_N	UPHY_RX0_N	HS_UPHY0_L0_RX_N

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
A24	GND	GND	–
A25	GND	GND	–
A26	UPHY_RX15_P	UPHY1_RX3_P	HS_UPHY1_L3_RX_P
A27	UPHY_RX15_N	UPHY1_RX3_N	HS_UPHY1_L3_RX_N
A28	GND	GND	–
A29	GND	GND	–
A30	UPHY_RX19_P	UPHY1_RX7_P	HS_UPHY1_L7_RX_P
A31	UPHY_RX19_N	UPHY1_RX7_N	HS_UPHY1_L7_RX_N
A32	GND	GND	–
A33	GND	GND	–
A34	UPHY_RX23_P	UPHY0_RX5_P	HS_UPHY0_L5_RX_P
A35	UPHY_RX23_N	UPHY0_RX5_N	HS_UPHY0_L5_RX_N
A36	GND	GND	–
A37	GND	GND	–
A38	PEX_C8_CLKREQ_N	XFI3_INT_N	GP181_PCIE3_CLKREQ_N
A39	PEX_C8_RST_N	XFI3_RST_N	GP182_PCIE3_RST_N
A40	GND	GND	–
A41	CSI2_D0_P	CSI_2_D0_P	HS_CSI2_D0_P
A42	CSI2_D0_N	CSI_2_D0_N	HS_CSI2_D0_N
A43	GND	GND	–
A44	CSI7_D0_P	CSI_7_D0_P	HS_CSI7_D0_P
A45	CSI7_D0_N	CSI_7_D0_N	HS_CSI7_D0_N
A46	GND	GND	–
A47	GPIO38	ETH_WOL_EN_STATUS	GP59
A48	GPIO37	XFI1_INT_N	GP60
A49	GND	GND	–
A50	HDMI_DP2_TX2_N	HDMI_DP0_TX2_N	HS_DISP0_HDMI_D0_DP2_N
A51	HDMI_DP2_TX2_P	HDMI_DP0_TX2_P	HS_DISP0_HDMI_D0_DP2_P
A52	GND	GND	–
A53	I2C5_CLK	I2C_GP9_CLK	GP81_I2C9_CLK
A54	GPIO17	GPIO_40PIN	GP56
A55	GPIO34	M2M_ALERT_N	GP69
A56	SPI1_MISO	SPI1_MISO	GP48_SPI1_MISO
A57	UART2_CTS	UART2_CTS	GP44_UART5_CTS_N
A58	GPIO20	3V3_DP_EN	GP205_DAP6_FS
A59	GPIO05	PCIE_12V_EN_N	GP203_DAP6_DOUT
A60	JTAG_TCK	JTAG_TCK	SF_JTAG_TCK

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
A61	SYSTEM_OC_N	SYSTEM_OC_N	GP03
A62	GPIO10	CAM_FRSYNC1	GP27
A63	GND	GND	–
B3	SYS_VIN_HV	VCC_SRC	–
B4	GND	GND	–
B5	RGMII_TXC	SNN_RGMII_TXC	GP147_RGMII0_TXC
B6	SDCARD_CLK	SDMMC1_CLK	GP129_SDMMC_A_CLK
B7	GND	GND	–
B8	GPIO11	CODEC_INT	GP166
B9	PEX_C1_RST_N	SNN_PCIE0_RST_N	GP176_PCIE0_RST_N
B10	RSVD	SNN_PWR_IRQ_N	–
B11	GND	GND	–
B12	UPHY_RX10_P	UPHY_RX10_P	HS_UPHY0_L6_RX_P
B13	UPHY_RX10_N	UPHY_RX10_N	HS_UPHY0_L6_RX_N
B14	GND	GND	–
B15	GND	GND	–
B16	UPHY_RX6_P	UPHY_RX6_P	HS_UPHY2_L4_RX_P
B17	UPHY_RX6_N	UPHY_RX6_N	HS_UPHY2_L4_RX_N
B18	GND	GND	–
B19	GND	GND	–
B20	UPHY_RX2_N	SNN_UPHY_RX2_N	HS_UPHY2_L0_RX_N
B21	UPHY_RX2_P	SNN_UPHY_RX2_P	HS_UPHY2_L0_RX_P
B22	GND	GND	–
B23	GND	GND	–
B24	UPHY_RX13_N	UPHY1_RX1_N	HS_UPHY1_L1_RX_N
B25	UPHY_RX13_P	UPHY1_RX1_P	HS_UPHY1_L1_RX_P
B26	GND	GND	–
B27	GND	GND	–
B28	UPHY_RX17_N	UPHY1_RX5_N	HS_UPHY1_L5_RX_N
B29	UPHY_RX17_P	UPHY1_RX5_P	HS_UPHY1_L5_RX_P
B30	GND	GND	–
B31	GND	GND	–
B32	UPHY_RX21_N	UPHY0_RX3_N	HS_UPHY0_L3_RX_N
B33	UPHY_RX21_P	UPHY0_RX3_P	HS_UPHY0_L3_RX_P
B34	GND	GND	–
B35	GND	GND	–
B36	PEX_C7_RST_N	PCIE1_RST_N	GP178_PCIE1_RST_N

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
B37	PEX_C7_CLKREQ_N	PCIE1_CLKREQ_N	GP177_PCIE1_CLKREQ_N
B38	GND	GND	–
B39	GND	GND	–
B40	RSVD	SNN_GP94_CAN2	–
B41	GND	GND	–
B42	CSI2_CLK_N	CSI_2_CLK_N	HS_CSI2_CLK_N
B43	CSI2_CLK_P	CSI_2_CLK_P	HS_CSI2_CLK_P
B44	GND	GND	–
B45	CSI7_CLK_P	CSI_7_CLK_P	HS_CSI7_CLK_P
B46	CSI7_CLK_N	CSI_7_CLK_N	HS_CSI7_CLK_N
B47	GND	GND	–
B48	RSVD	UART7_TXD	–
B49	RSVD	UART7_RXD	–
B50	GND	GND	–
B51	HDMI_DP2_TX1_P	HDMI_DP0_TX1_P	HS_DISP0_HDMI_D1_DP1_P
B52	HDMI_DP2_TX1_N	HDMI_DP0_TX1_N	HS_DISP0_HDMI_D1_DP1_N
B53	GND	GND	–
B54	WDT_RESET_OUT_N	SNN_WDT_RESET_OUT_N	GP63
B55	GPIO30	M2E_ALERT_N	GP02
B56	SPI1_CS1_N	SPI1_CS1_40PIN	GP51_SPI1_CS1_N
B57	GND	GND	–
B58	GPIO21	SD_POWER_EN	GP202_DAP6_CLK
B59	GPIO04	I2C_GP3_PEX_EN_N	GP204_DAP6_DIN
B60	JTAG_TDI	JTAG_TDI	SF_JTAG_TDI
B61	CAN1_DIN	CAN1_DIN	GP20_CAN1_DIN
B62	GPIO08	GPIO8_DMIC3_DAT_40PIN	GP26
B63	SYS_VIN_HV	VCC_SRC	–
C1	SYS_VIN_HV	VCC_SRC	–
C2	SYS_VIN_HV	VCC_SRC	–
C3	GND	GND	–
C4	RGMII_RD0	SNN_RGMII_RD0	GP153_RGMII0_RD0
C5	RGMII_RXC	SNN_RGMII_RXC	GP158_RGMII0_RXC
C6	UFS0_RST_N	UFS0_RST_N	GP174_UFS_A_RST_N
C7	I2S1_SDOUT	I2S1_DOUT	GP170
C8	PEX_C5_CLKREQ_N	PCIE5_CLKREQ_N	GP210_PCIE5_CLKREQ_N
C9	GND	GND	–
C10	USB1_N	USB2_1_N	HS_USB0_P1_N

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
C11	USB1_P	USB2_1_P	HS_USB0_P1_P
C12	GND	GND	–
C13	GND	GND	–
C14	UPHY_RX9_N	UPHY_RX9_N	HS_UPHY2_L7_RX_N
C15	UPHY_RX9_P	UPHY_RX9_P	HS_UPHY2_L7_RX_P
C16	GND	GND	–
C17	GND	GND	–
C18	UPHY_RX5_N	SNN_UPHY_RX5_N	HS_UPHY2_L3_RX_N
C19	UPHY_RX5_P	SNN_UPHY_RX5_P	HS_UPHY2_L3_RX_P
C20	GND	GND	–
C21	GND	GND	–
C22	UPHY_RX1_N	UPHY_RX1_N	HS_UPHY0_L1_RX_N
C23	UPHY_RX1_P	UPHY_RX1_P	HS_UPHY0_L1_RX_P
C24	GND	GND	–
C25	GND	GND	–
C26	UPHY_RX14_N	UPHY1_RX2_N	HS_UPHY1_L2_RX_N
C27	UPHY_RX14_P	UPHY1_RX2_P	HS_UPHY1_L2_RX_P
C28	GND	GND	–
C29	GND	GND	–
C30	UPHY_RX18_N	UPHY1_RX6_N	HS_UPHY1_L6_RX_N
C31	UPHY_RX18_P	UPHY1_RX6_P	HS_UPHY1_L6_RX_P
C32	GND	GND	–
C33	GND	GND	–
C34	UPHY_RX20_P	UPHY0_RX2_P	HS_UPHY0_L2_RX_P
C35	UPHY_RX20_N	UPHY0_RX2_N	HS_UPHY0_L2_RX_N
C36	GND	GND	–
C37	GND	GND	–
C38	UPHY_REFCLK4_N	SNN_UPHY1_REFCLK1_N	HS_UPHY1_REFCLK1_N
C39	UPHY_REFCLK4_P	SNN_UPHY1_REFCLK1_P	HS_UPHY1_REFCLK1_P
C40	GND	GND	–
C41	CSI2_D1_N	CSI_2_D1_N	HS_CSI2_D1_N
C42	CSI2_D1_P	CSI_2_D1_P	HS_CSI2_D1_P
C43	GND	GND	–
C44	CSI5_CLK_P	CSI_5_CLK_P	HS_CSI5_CLK_P
C45	CSI5_CLK_N	CSI_5_CLK_N	HS_CSI5_CLK_N
C46	GND	GND	–
C47	CSI7_D1_P	CSI_7_D1_P	HS_CSI7_D1_P

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
C48	CSI7_D1_N	CSI_7_D1_N	HS_CSI7_D1_N
C49	GND	GND	–
C50	HDMI_DP2_TX3_N	HDMI_DP0_TX3_N	HS_DISP0_HDMI_CK_DP3_N
C51	HDMI_DP2_TX3_P	HDMI_DP0_TX3_P	HS_DISP0_HDMI_CK_DP3_P
C52	GND	GND	–
C53	I2C5_DAT	I2C_GP9_DAT	GP82_I2C9_DAT
C54	GPIO33	GPIO33_XFI1_MDIO	GP87_XFI1_MDIO
C55	GPIO18	PCIE_REFCLK_SEL	GP64
C56	UART2_RX	UART2_RXD	GP42_UART5_RXD
C57	SPI3_CS0_N	XFI0_INT_N	GP39_SPI3_CS0_N
C58	UART2_TX	UART2_TXD	GP41_UART5_TXD_DDRCODE1
C59	I2S3_SCLK	I2S4_SCLK	GP206_DAP4_CLK
C60	I2S3_FS	I2S4_FS	GP209_DAP4_FS
C61	GPIO09	GPIO9_DMIC3_CLK_40PIN	GP25
C62	GND	GND	–
C63	SYS_VIN_HV	VCC_SRC	–
C64	SYS_VIN_HV	VCC_SRC	–
C65	SYS_VIN_HV	VCC_SRC	–
D1	SYS_VIN_HV	VCC_SRC	–
D2	SYS_VIN_HV	VCC_SRC	–
D3	SYS_VIN_HV	VCC_SRC	–
D4	GND	GND	–
D5	RGMII_RX_CTL	SNN_RGMII_RX_CTL	GP157_RGMII0_RX_CTL
D6	SDCARD_D3	SDMMC1_D3	GP134_SDMMC_A3
D7	GND	GND	–
D8	I2S1_FS	I2S1_FS	GP172
D9	PEX_C1_CLKREQ_N	SNN_PCIE0_CLKREQ_N	GP175_PCIE0_CLKREQ_N
D10	PEX_C0_RST_N	SNN_PCIE7_RST_N	GP188_PCIE7_RST_N
D11	GND	GND	–
D12	UPHY_RX11_P	UPHY_RX11_P	HS_UPHY0_L7_RX_P
D13	UPHY_RX11_N	UPHY_RX11_N	HS_UPHY0_L7_RX_N
D14	GND	GND	–
D15	GND	GND	–
D16	UPHY_RX7_P	UPHY_RX7_P	HS_UPHY2_L5_RX_P
D17	UPHY_RX7_N	UPHY_RX7_N	HS_UPHY2_L5_RX_N
D18	GND	GND	–
D19	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
D20	UPHY_RX3_P	SNN_UPHY_RX3_P	HS_UPHY2_L1_RX_P
D21	UPHY_RX3_N	SNN_UPHY_RX3_N	HS_UPHY2_L1_RX_N
D22	GND	GND	–
D23	GND	GND	–
D24	UPHY_RX12_P	UPHY1_RX0_P	HS_UPHY1_L0_RX_P
D25	UPHY_RX12_N	UPHY1_RX0_N	HS_UPHY1_L0_RX_N
D26	GND	GND	–
D27	GND	GND	–
D28	UPHY_RX16_P	UPHY1_RX4_P	HS_UPHY1_L4_RX_P
D29	UPHY_RX16_N	UPHY1_RX4_N	HS_UPHY1_L4_RX_N
D30	GND	GND	–
D31	GND	GND	–
D32	UPHY_RX22_N	UPHY0_RX4_N	HS_UPHY0_L4_RX_N
D33	UPHY_RX22_P	UPHY0_RX4_P	HS_UPHY0_L4_RX_P
D34	GND	GND	–
D35	GND	GND	–
D36	RSVD	SNN_GP201	–
D37	PMIC_BBATT	VDD_BBAT	–
D38	GND	GND	–
D39	GND	GND	–
D40	RSVD	SNN_GP93_CAN2	–
D41	GND	GND	–
D42	CSI5_D0_P	CSI_5_D0_P	HS_CSI5_D0_P
D43	CSI5_D0_N	CSI_5_D0_N	HS_CSI5_D0_N
D44	GND	GND	–
D45	CSI5_D1_N	CSI_5_D1_N	HS_CSI5_D1_N
D46	CSI5_D1_P	CSI_5_D1_P	HS_CSI5_D1_P
D47	GND	GND	–
D48	PEX_CLK6_N	UPHY0_SF_PCIE1_CLK_N	SF_PCIE1_CLK_N
D49	PEX_CLK6_P	UPHY0_SF_PCIE1_CLK_P	SF_PCIE1_CLK_P
D50	GND	GND	–
D51	HDMI_DP2_TX0_P	HDMI_DP0_TX0_P	HS_DISP0_HDMI_D2_DP0_P
D52	HDMI_DP2_TX0_N	HDMI_DP0_TX0_N	HS_DISP0_HDMI_D2_DP0_N
D53	GND	GND	–
D54	GPIO03	GPIO03_XFI2_MDC	GP84_XFI2_MDC
D55	SPI1_MOSI	SPI1_MOSI	GP49_SPI1_MOSI
D56	SPI3_MISO	XFI0_RST_N	GP37_SPI3_MISO

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
D57	GND	GND	–
D58	JTAG_TDO	JTAG_TDO	SF_JTAG_TDO
D59	CAN0_DOUT	CAN0_DOUT	GP17_CAN0_DOUT
D60	SPI2_CS0_N	CAM_INT4	GP09_SPI2_CS_N
D61	I2C4_CLK	I2C_GP8_CLK	GP15_I2C8_CLK
D62	SPI2_MISO	CAM_INT2	GP07_SPI2_MISO
D63	GND	GND	–
D64	SYS_VIN_HV	VCC_SRC	–
D65	SYS_VIN_HV	VCC_SRC	–
E1	SYS_VIN_HV	VCC_SRC	–
E2	SYS_VIN_HV	VCC_SRC	–
E3	GND	GND	–
E4	I2S2_FS	I2S2_FS	GP125
E5	RGMII_RD3	SNN_RGMII_RD3	GP156_RGMII0_RD3
E6	RGMII_SMA_MDC	RGMII_SMA_MDC	GP160_RGMII0_SMA_MDC
E7	RGMII_SMA_MDIO	RGMII_SMA_MDIO	GP159_RGMII0_SMA_MDIO
E8	SDCARD_D0	SDMMC1_D0	GP131_SDMMC_A0
E9	GND	GND	–
E10	GPIO12	CAM_VDD_SYS_EN	GP168
E11	PEX_C0_CLKREQ_N	SNN_PCIE7_CLKREQ_N	GP187_PCIE7_CLKREQ_N
E12	GND	GND	–
E13	GND	GND	–
E14	PEX_CLK0_N	SNN_PCIE7_CLK_N	SF_PCIE7_CLK_N
E15	PEX_CLK0_P	SNN_PCIE7_CLK_P	SF_PCIE7_CLK_P
E16	GND	GND	–
E17	GND	GND	–
E18	PEX_CLK2_N	SNN_PCIE8_CLK_N	SF_PCIE8_CLK_N
E19	PEX_CLK2_P	SNN_PCIE8_CLK_P	SF_PCIE8_CLK_P
E20	GND	GND	–
E21	GND	GND	–
E22	PEX_CLK4_N	PCIE4_CLK_N	SF_PCIE4_CLK_N
E23	PEX_CLK4_P	PCIE4_CLK_P	SF_PCIE4_CLK_P
E24	GND	GND	–
E25	GND	GND	–
E26	UPHY_REFCLK1_N	SNN_UPHY2_REFCLK1_N	HS_UPHY2_REFCLK1_N
E27	UPHY_REFCLK1_P	SNN_UPHY2_REFCLK1_P	HS_UPHY2_REFCLK1_P
E28	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
E29	GND	GND	–
E30	UPHY_REFCLK0_P	UPHY1_REFCLK0_P	HS_UPHY1_REFCLK0_P
E31	UPHY_REFCLK0_N	UPHY1_REFCLK0_N	HS_UPHY1_REFCLK0_N
E32	GND	GND	–
E33	GND	GND	–
E34	RSVD	SNN_GP198_FSI_SPI7_CS0	–
E35	RSVD	SNN_GP197_FSI_SPI7_MOSI	–
E36	GND	GND	–
E37	GND	GND	–
E38	CSI0_D1_N	CSI_0_D1_N	HS_CSI0_D1_N
E39	CSI0_D1_P	CSI_0_D1_P	HS_CSI0_D1_P
E40	GND	GND	–
E41	CSI0_D0_N	CSI_0_D0_N	HS_CSI0_D0_N
E42	CSI0_D0_P	CSI_0_D0_P	HS_CSI0_D0_P
E43	GND	GND	–
E44	CSI3_D0_N	CSI_3_D0_N	HS_CSI3_D0_N
E45	CSI3_D0_P	CSI_3_D0_P	HS_CSI3_D0_P
E46	GND	GND	–
E47	CSI4_D1_P	CSI_4_D1_P	HS_CSI4_D1_P
E48	CSI4_D1_N	CSI_4_D1_N	HS_CSI4_D1_N
E49	GND	GND	–
E50	RSVD	SNN_GP215	–
E51	RSVD	SNN_GP214	–
E52	GND	GND	–
E53	I2C3_DAT	I2C_GP3_DAT	GP55_I2C3_DAT
E54	FAN_TACH	FAN_TACH	GP62
E55	SPI1_CS0_N	SPI1_CS0	GP50_SPI1_CS0_N
E56	SPI3_CS1_N	I2C_INT_CCG4	GP40_SPI3_CS1_N
E57	GND	GND	–
E58	JTAG_TMS	JTAG_TMS	SF_JTAG_TMS
E59	GPIO06	CAM_FRSYNC3	GP21
E60	I2C4_DAT	I2C_GP8_DAT	GP16_I2C8_DAT
E61	SPI2_CLK	CAM_INT1	GP06_SPI2_CLK
E62	GND	GND	–
E63	SYS_VIN_HV	VCC_SRC	–
E64	SYS_VIN_HV	VCC_SRC	–
E65	SYS_VIN_HV	VCC_SRC	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
F1	SYS_VIN_HV	VCC_SRC	–
F2	SYS_VIN_HV	VCC_SRC	–
F3	SYS_VIN_HV	VCC_SRC	–
F4	GND	GND	–
F5	I2S2_DOUT	I2S2_DOUT	GP123
F6	I2S2_DIN	I2S2_DIN	GP124
F7	GND	GND	–
F8	SDCARD_D1	SDMMC1_D1	GP132_SDMMC_A1
F9	GPIO16	CAM1_RST	GP162_SPI5_MISO
F10	GPIO15	CAM1_PWDN	GP161_SPI5_CLK
F11	GND	GND	–
F12	USB0_P	USB2_0_P	HS_USB0_P0_P
F13	USB0_N	USB2_0_N	HS_USB0_P0_N
F14	GND	GND	–
F15	GND	GND	–
F16	PEX_CLK1_P	SNN_PCIE0_CLK_P	SF_PCIE0_CLK_P
F17	PEX_CLK1_N	SNN_PCIE0_CLK_N	SF_PCIE0_CLK_N
F18	GND	GND	–
F19	GND	GND	–
F20	PEX_CLK3_P	SNN_PCIE10_CLK_P	SF_PCIE10_CLK_P
F21	PEX_CLK3_N	SNN_PCIE10_CLK_N	SF_PCIE10_CLK_N
F22	GND	GND	–
F23	GND	GND	–
F24	PEX_CLK5_P	PCIE5_CLK_P	SF_PCIE5_CLK_P
F25	PEX_CLK5_N	PCIE5_CLK_N	SF_PCIE5_CLK_N
F26	GND	GND	–
F27	GND	GND	–
F28	UPHY_REFCLK2_P	UPHY2_REFCLK2_P	HS_UPHY2_REFCLK2_P
F29	UPHY_REFCLK2_N	UPHY2_REFCLK2_N	HS_UPHY2_REFCLK2_N
F30	GND	GND	–
F31	GND	GND	–
F32	UPHY_REFCLK3_P	SNN_PCIE6_CLK_P	SF_PCIE6_CLK_P
F33	UPHY_REFCLK3_N	SNN_PCIE6_CLK_N	SF_PCIE6_CLK_N
F34	GND	GND	–
F35	GND	GND	–
F36	RSVD	SNN_GP196_FSI_SPI7_MISO	–
F37	RSVD	SNN_GP195_FSI_SPI7_CLK	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
F38	GND	GND	–
F39	GND	GND	–
F40	RSVD	SNN_GP92_CAN2	–
F41	GND	GND	–
F42	CSI0_CLK_N	CSI_0_CLK_N	HS_CSI0_CLK_N
F43	CSI0_CLK_P	CSI_0_CLK_P	HS_CSI0_CLK_P
F44	GND	GND	–
F45	CSI3_CLK_N	CSI_3_CLK_N	HS_CSI3_CLK_N
F46	CSI3_CLK_P	CSI_3_CLK_P	HS_CSI3_CLK_P
F47	GND	GND	–
F48	CSI4_CLK_P	CSI_4_CLK_P	HS_CSI4_CLK_P
F49	CSI4_CLK_N	CSI_4_CLK_N	HS_CSI4_CLK_N
F50	GND	GND	–
F51	DP0_AUX_CH_N	SNN_I2C_GP7_DAT	GP79_I2C7_DAT
F52	DP0_AUX_CH_P	SNN_I2C_GP7_CLK	GP78_I2C7_CLK
F53	I2C3_CLK	I2C_GP3_CLK	GP54_I2C3_CLK
F54	GPIO22	XFI2_INT_N	GP45_USB_VBUS_EN0
F55	SPI3_CLK	M2E_BT_DISABLE_N	GP36_SPI3_CLK
F56	GPIO36	CAM_AVDD_EN	GP61
F57	GND	GND	–
F58	CAN0_DIN	CAN0_DIN	GP18_CAN0_DIN
F59	GPIO07	CAM_FRSYNC2	GP24
F60	SPI2_MOSI	CAM_INT3	GP08_SPI2_MOSI
F61	VCOMP_ALERT_N	SNN_VCOMP_ALERT_N	GP01
F62	GND	GND	–
F63	SYS_VIN_HV	VCC_SRC	–
F64	SYS_VIN_HV	VCC_SRC	–
F65	SYS_VIN_HV	VCC_SRC	–
G1	SYS_VIN_HV	VCC_SRC	–
G2	SYS_VIN_HV	VCC_SRC	–
G3	GND	GND	–
G4	I2S2_CLK	I2S2_SCLK	GP122
G5	RGMII_TD1	SNN_RGMII_TD1	GP149_RGMII0_TD1
G6	RGMII_TD3	SNN_RGMII_TD3	GP151_RGMII0_TD3
G7	GPIO13	CAM_FRSYNC4	GP163_SPI5_MOSI
G8	PEX_C4_CLKREQ_N	PCIE4_CLKREQ_N	GP183_PCIE4_CLKREQ_N
G9	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
G10	USB3_N	USB2_3_N	HS_USB0_P3_N
G11	USB3_P	USB2_3_P	HS_USB0_P3_P
G12	GND	GND	–
G13	GND	GND	–
G14	UPHY_TX9_N	UPHY_TX9_N	HS_UPHY2_L7_TX_N
G15	UPHY_TX9_P	UPHY_TX9_P	HS_UPHY2_L7_TX_P
G16	GND	GND	–
G17	GND	GND	–
G18	UPHY_TX5_N	SNN_UPHY_TX5_N	HS_UPHY2_L3_TX_N
G19	UPHY_TX5_P	SNN_UPHY_TX5_P	HS_UPHY2_L3_TX_P
G20	GND	GND	–
G21	GND	GND	–
G22	UPHY_TX1_N	UPHY_TX1_N	HS_UPHY0_L1_TX_N
G23	UPHY_TX1_P	UPHY_TX1_P	HS_UPHY0_L1_TX_P
G24	GND	GND	–
G25	GND	GND	–
G26	UPHY_TX14_N	UPHY1_TX2_N	HS_UPHY1_L2_TX_N
G27	UPHY_TX14_P	UPHY1_TX2_P	HS_UPHY1_L2_TX_P
G28	GND	GND	–
G29	GND	GND	–
G30	UPHY_TX18_N	UPHY1_TX6_N	HS_UPHY1_L6_TX_N
G31	UPHY_TX18_P	UPHY1_TX6_P	HS_UPHY1_L6_TX_P
G32	GND	GND	–
G33	GND	GND	–
G34	UPHY_TX21_N	UPHY0_TX3_N	HS_UPHY0_L3_TX_N
G35	UPHY_TX21_P	UPHY0_TX3_P	HS_UPHY0_L3_TX_P
G36	GND	GND	–
G37	GND	GND	–
G38	RSVD	SNN_CAN2_DOUT	–
G39	RSVD	SNN_CAN2_DIN	–
G40	GND	GND	–
G41	CSI1_D0_P	CSI_1_D0_P	HS_CSI1_D0_P
G42	CSI1_D0_N	CSI_1_D0_N	HS_CSI1_D0_N
G43	GND	GND	–
G44	CSI3_D1_P	CSI_3_D1_P	HS_CSI3_D1_P
G45	CSI3_D1_N	CSI_3_D1_N	HS_CSI3_D1_N
G46	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
G47	CSI4_D0_N	CSI_4_D0_N	HS_CSI4_D0_N
G48	CSI4_D0_P	CSI_4_D0_P	HS_CSI4_D0_P
G49	GND	GND	–
G50	RSVD	SNN_RSVD_3	–
G51	RSVD	SNN_RSVD_4	–
G52	GND	GND	–
G53	DP2_AUX_CH_P	DP2_AUX_CH_P_I2C6_CLK	SF_DPAUX01_P
G54	DP2_AUX_CH_N	DP2_AUX_CH_N_I2C6_DAT	SF_DPAUX01_N
G55	GPIO23	M2E_WIFI_WAKE	GP46_USB_VBUS_EN1
G56	SPI3_MOSI	XFI1_RST_N	GP38_SPI3_MOSI
G57	GND	GND	–
G58	UART2_RTS	UART2_RTS	GP43_UART5_RTS_N_DDRCODE0
G59	RSVD	SNN_TEMP_THERM	–
G60	NVDBG_SEL	NVDBG_SEL	SF_NVDBG_SEL
G61	JTAG_TRST_N	JTAG_TRST_N	SF_JTAG_TRST_N
G62	GND	GND	–
G63	SYS_VIN_HV	VCC_SRC	–
G64	SYS_VIN_HV	VCC_SRC	–
G65	SYS_VIN_HV	VCC_SRC	–
H1	SYS_VIN_HV	VCC_SRC	–
H2	SYS_VIN_HV	VCC_SRC	–
H3	SYS_VIN_HV	VCC_SRC	–
H4	GND	GND	–
H5	ENET_RST_N	SNN_ENET_RST_N	GP112
H6	RGMII_RD2	SNN_RGMII_RD2	GP155_RGMII0_RD2
H7	GND	GND	–
H8	I2S1_SDIN	I2S1_DIN	GP171
H9	MCLK01	MCLK01_AUDIO_MCLK	GP167
H10	PEX_C5_RST_N	PCIE5_RST_N	GP211_PCIE5_RST_N
H11	GND	GND	–
H12	UPHY_TX11_P	UPHY_TX11_P	HS_UPHY0_L7_TX_P
H13	UPHY_TX11_N	UPHY_TX11_N	HS_UPHY0_L7_TX_N
H14	GND	GND	–
H15	GND	GND	–
H16	UPHY_TX7_P	UPHY_TX7_P	HS_UPHY2_L5_TX_P
H17	UPHY_TX7_N	UPHY_TX7_N	HS_UPHY2_L5_TX_N
H18	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
H19	GND	GND	–
H20	UPHY_TX3_P	SNN_UPHY_TX3_P	HS_UPHY2_L1_TX_P
H21	UPHY_TX3_N	SNN_UPHY_TX3_N	HS_UPHY2_L1_TX_N
H22	GND	GND	–
H23	GND	GND	–
H24	UPHY_TX12_P	UPHY1_TX0_P	HS_UPHY1_L0_TX_P
H25	UPHY_TX12_N	UPHY1_TX0_N	HS_UPHY1_L0_TX_N
H26	GND	GND	–
H27	GND	GND	–
H28	UPHY_TX16_P	UPHY1_TX4_P	HS_UPHY1_L4_TX_P
H29	UPHY_TX16_N	UPHY1_TX4_N	HS_UPHY1_L4_TX_N
H30	GND	GND	–
H31	GND	GND	–
H32	UPHY_TX23_P	UPHY0_TX5_P	HS_UPHY0_L5_TX_P
H33	UPHY_TX23_N	UPHY0_TX5_N	HS_UPHY0_L5_TX_N
H34	GND	GND	–
H35	GND	GND	–
H36	RSVD	SNN_CAN3_DIN	–
H37	RSVD	SNN_CAN3_DOUT	–
H38	GND	GND	–
H39	GND	GND	–
H40	MID1	SNN_MID1	–
H41	GND	GND	–
H42	CSI1_CLK_N	CSI_1_CLK_N	HS_CSI1_CLK_N
H43	CSI1_CLK_P	CSI_1_CLK_P	HS_CSI1_CLK_P
H44	GND	GND	–
H45	CSI6_D1_N	CSI_6_D1_N	HS_CSI6_D1_N
H46	CSI6_D1_P	CSI_6_D1_P	HS_CSI6_D1_P
H47	GND	GND	–
H48	RSVD	SNN_RSVD_1	–
H49	RSVD	SNN_RSVD_2	–
H50	GND	GND	–
H51	GPIO26	GPIO26_XFI0_MDC	GP86_XFI0_MDC
H52	GPIO27	PWM2_40PIN	GP88_PWM1
H53	MCLK03	MCLK03_MCLK	GP53_CLK2
H54	UART1_CTS	UART1_CTS	GP73_UART1_CTS_N
H55	MCLK04	MCLK04_MCLK	GP65

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
H56	GND	GND	–
H57	UART5_CTS	UART5_CTS	GP35_UART2_CTS_N
H58	UART5_RX	UART5_RXD	GP33_UART2_RXD
H59	NVJTAG_SEL	NVJTAG_SEL	SF_NVJTAG_SEL
H60	GPIO31	PCIE_PRSNT	GP186
H61	CAN1_DOUT	CAN1_DOUT	GP19_CAN1_DOUT
H62	UART3_TX_DEBUG	UART3_TXD_DEBUG	GP11_UART3_TXD
H63	GND	GND	–
H64	SYS_VIN_HV	VCC_SRC	–
H65	SYS_VIN_HV	VCC_SRC	–
J1	SYS_VIN_HV	VCC_SRC	–
J2	SYS_VIN_HV	VCC_SRC	–
J3	GND	GND	–
J4	GPIO01	M2E_WIFI_DISABLE_N	GP110
J5	ENET_INT	SNN_ENET_INT	GP111
J6	RGMII_TD0	SNN_RGMII_TD0	GP148_RGMII0_TD0
J7	RGMII_TD2	SNN_RGMII_TD2	GP150_RGMII0_TD2
J8	GND	GND	–
J9	PEX_C4_RST_N	PCIE4_RST_N	GP184_PCIE4_RST_N
J10	PEX_C3_CLKREQ_N	SNN_PCIE10_CLKREQ_N	GP193_PCIE10_CLKREQ_N
J11	PEX_C2_CLKREQ_N	SNN_PCIE8_CLKREQ_N	GP189_PCIE8_CLKREQ_N
J12	GND	GND	–
J13	GND	GND	–
J14	UPHY_TX8_P	UPHY_TX8_P	HS_UPHY2_L6_TX_P
J15	UPHY_TX8_N	UPHY_TX8_N	HS_UPHY2_L6_TX_N
J16	GND	GND	–
J17	GND	GND	–
J18	UPHY_TX4_P	SNN_UPHY_TX4_P	HS_UPHY2_L2_TX_P
J19	UPHY_TX4_N	SNN_UPHY_TX4_N	HS_UPHY2_L2_TX_N
J20	GND	GND	–
J21	GND	GND	–
J22	UPHY_TX0_P	UPHY_TX0_P	HS_UPHY0_L0_TX_P
J23	UPHY_TX0_N	UPHY_TX0_N	HS_UPHY0_L0_TX_N
J24	GND	GND	–
J25	GND	GND	–
J26	UPHY_TX15_P	UPHY1_TX3_P	HS_UPHY1_L3_TX_P
J27	UPHY_TX15_N	UPHY1_TX3_N	HS_UPHY1_L3_TX_N

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
J28	GND	GND	–
J29	GND	GND	–
J30	UPHY_TX19_P	UPHY1_TX7_P	HS_UPHY1_L7_TX_P
J31	UPHY_TX19_N	UPHY1_TX7_N	HS_UPHY1_L7_TX_N
J32	GND	GND	–
J33	GND	GND	–
J34	UPHY_TX22_N	UPHY0_TX4_N	HS_UPHY0_L4_TX_N
J35	UPHY_TX22_P	UPHY0_TX4_P	HS_UPHY0_L4_TX_P
J36	GND	GND	–
J37	GND	GND	–
J38	RSVD	SNN_GP97_CAN3	–
J39	RSVD	SNN_GP98_CAN3	–
J40	GND	GND	–
J41	CSI1_D1_P	CSI_1_D1_P	HS_CSI1_D1_P
J42	CSI1_D1_N	CSI_1_D1_N	HS_CSI1_D1_N
J43	GND	GND	–
J44	CSI6_CLK_P	CSI_6_CLK_P	HS_CSI6_CLK_P
J45	CSI6_CLK_N	CSI_6_CLK_N	HS_CSI6_CLK_N
J46	GND	GND	–
J47	RSVD	SNN_RSVD_6	–
J48	RSVD	SNN_RSVD_5	–
J49	GND	GND	–
J50	HDMI_CEC	HDMI_CEC	GP05_HDMI_CEC
J51	GPIO24	GPIO24_XFI2_MDIO_CVM	GP83_XFI2_MDIO
J52	DP1_AUX_CH_P	XFI2_RST_N	GP75_I2C4_CLK
J53	DP1_AUX_CH_N	XFI_DETECT_N	GP76_I2C4_DAT
J54	MCLK02	MCLK02_MCLK	GP52_CLK1
J55	GPIO32	M2E_BT_WAKE	GP58
J56	GND	GND	–
J57	SPI1_CLK	SPI1_SCK	GP47_SPI1_CLK
J58	UART5_TX	UART5_TXD	GP32_UART2_TXD
J59	I2S3_DIN	I2S4_DIN	GP208_DAP4_DIN
J60	MODULE_SLEEP_N	SOC_PWR_REQ	SF_PWR_SOC_EN
J61	I2C2_CLK	I2C_GP2_CLK	GP13_I2C2_CLK
J62	RSVD	MOD_TEMP_SHDN_EN_N	–
J63	SYS_VIN_HV	VCC_SRC	–
J64	SYS_VIN_HV	VCC_SRC	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
J65	SYS_VIN_HV	VCC_SRC	–
K3	SYS_VIN_HV	VCC_SRC	–
K4	GND	GND	–
K5	I2C1_CLK	I2C_GP1_CLK	GP126_I2C1_CLK
K6	RGMII_RD1	SNN_RGMII_RD1	GP154_RGMII0_RD1
K7	RGMII_TX_CTL	SNN_RGMII_TX_CTL	GP152_RGMII0_TX_CTL
K8	GND	GND	–
K9	PEX_C3_RST_N	SNN_PCIE10_RST_N	GP194_PCIE10_RST_N
K10	PEX_C2_RST_N	SNN_PCIE8_RST_N	GP190_PCIE8_RST_N
K11	GND	GND	–
K12	UPHY_TX10_N	UPHY_TX10_N	HS_UPHY0_L6_TX_N
K13	UPHY_TX10_P	UPHY_TX10_P	HS_UPHY0_L6_TX_P
K14	GND	GND	–
K15	GND	GND	–
K16	UPHY_TX6_N	UPHY_TX6_N	HS_UPHY2_L4_TX_N
K17	UPHY_TX6_P	UPHY_TX6_P	HS_UPHY2_L4_TX_P
K18	GND	GND	–
K19	GND	GND	–
K20	UPHY_TX2_N	SNN_UPHY_TX2_N	HS_UPHY2_L0_TX_N
K21	UPHY_TX2_P	SNN_UPHY_TX2_P	HS_UPHY2_L0_TX_P
K22	GND	GND	–
K23	GND	GND	–
K24	UPHY_TX13_N	UPHY1_TX1_N	HS_UPHY1_L1_TX_N
K25	UPHY_TX13_P	UPHY1_TX1_P	HS_UPHY1_L1_TX_P
K26	GND	GND	–
K27	GND	GND	–
K28	UPHY_TX17_N	UPHY1_TX5_N	HS_UPHY1_L5_TX_N
K29	UPHY_TX17_P	UPHY1_TX5_P	HS_UPHY1_L5_TX_P
K30	GND	GND	–
K31	GND	GND	–
K32	UPHY_TX20_P	UPHY0_TX2_P	HS_UPHY0_L2_TX_P
K33	UPHY_TX20_N	UPHY0_TX2_N	HS_UPHY0_L2_TX_N
K34	GND	GND	–
K35	GND	GND	–
K36	RSVD	SNN_GP99_CAN3	–
K37	RSVD	SNN_GP100_SOC_ERROR_N	–
K38	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
K39	GND	GND	–
K40	MID0	SNN_MID0	–
K41	GND	GND	–
K42	GND	GND	–
K43	CSI6_D0_N	CSI_6_D0_N	HS_CSI6_D0_N
K44	CSI6_D0_P	CSI_6_D0_P	HS_CSI6_D0_P
K45	GND	GND	–
K46	RSVD	SNN_RSVD_8	–
K47	RSVD	SNN_RSVD_7	–
K48	GND	GND	–
K49	GPIO25	GPIO25_XFI0_MDIO	GP85_XFI0_MDIO
K50	DP2_HPD	DP2_HPD_CH0_HPD	GP74_HPD0_N
K51	DP1_HPD	DP1_HPD_GP77_XFI3_MDIO	GP77_XFI3_MDIO
K52	DP0_HPD	DP2_HPD_GP80_XFI3_MDC	GP80_XFI3_MDC
K53	UART1_TX	UART1_TXD	GP70_UART1_TXD_BOOT2_STRAP
K54	UART1_RX	UART1_RXD	GP71_UART1_RXD
K55	GND	GND	–
K56	GPIO19	GPIO19_XFI1_MDC	GP89_XFI1_MDC
K57	PWM01	PWM01_BKLIGHT_GMSL_INT3_GP68	GP68
K58	UART5_RTS	UART5_RTS	GP34_UART2_RTS_N
K59	I2S3_DOUT	I2S4_DOUT	GP207_DAP4_DOUT
K60	UART3_RX_DEBUG	UART3_RXD_DEBUG	GP12_UART3_RXD
K61	I2C2_DAT	I2C_GP2_DAT	GP14_I2C2_DAT
K62	FAN_PWM	FAN_PWM	GP31_PWM3
K63	GND	GND	–
L3	GND	GND	–
L4	UART4_RTS	CAM_ERROR4	GP120_UART4_RTS_N_BOOT0_STRAP
L5	UART4_TX	CAM0_RST	GP118_UART4_TXD_BOOT1_STRAP
L6	GPIO02	SD_DET_N	GP114
L7	GND	GND	–
L8	I2C1_DAT	I2C_GP1_DAT	GP127_I2C1_DAT
L9	GPIO28	CAM_ERROR2	GP116
L10	FORCE_RECOVERY_N	FORCE_RECOVERY_N	GP107_RECOVERY0_STRAP
L11	SLEEP_REQ_N	STANDBY_REQ_N_GP109	GP109
L12	GND	GND	–
L13	GND	GND	–
L14	I2S1_CLK	I2S1_SCLK	GP169

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
L15	GPIO14	CAM_ERROR1	GP164_SPI5_CS0
L16	GND	GND	–
L17	GND	GND	–
L18	PEX_C6_RST_N	SNN_PCIE6_RST_N	GP213_PCIE6_RST_N
L19	PEX_C6_CLKREQ_N	SNN_PCIE6_CLKREQ_N	GP212_PCIE6_CLKREQ_N
L20	GND	GND	–
L21	GND	GND	–
L22	SYS_VIN_MV	VDD_5V	–
L23	SYS_VIN_MV	VDD_5V	–
L24	GND	GND	–
L25	GND	GND	–
L26	SYS_VIN_MV	VDD_5V	–
L27	SYS_VIN_MV	VDD_5V	–
L28	GND	GND	–
L29	GND	GND	–
L30	SYS_VIN_MV	VDD_5V	–
L31	SYS_VIN_MV	VDD_5V	–
L32	GND	GND	–
L33	GND	GND	–
L34	SYS_VIN_MV	VDD_5V	–
L35	SYS_VIN_MV	VDD_5V	–
L36	GND	GND	–
L37	GND	GND	–
L38	SYS_VIN_MV	VDD_5V	–
L39	SYS_VIN_MV	VDD_5V	–
L40	GND	GND	–
L41	RSVD	SNN_VM_EN1_N	–
L42	RSVD	SNN_VM_EN0_N	–
L43	GND	GND	–
L44	RSVD	VM_I2C_CLK	–
L45	RSVD	VM_I2C_DAT	–
L46	GND	GND	–
L47	RSVD	SNN_VM_INT_N	–
L48	UART4_RX	PCIE_3V3_EN	GP119_UART4_RXD
L49	UART4_CTS	CAM0_PWDN	GP121_UART4_CTS_N
L50	GPIO35	PWM3_40PIN	GP115
L51	UART1_RTS	UART1_RTS	GP72_UART1_RTS_N

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
L52	MODULE_SHDN_N	MOD_SHUTDOWN_N	GP67
L53	RSVD	SAFE_3V3	–
L54	MODULE_POWER_ON	MODULE_POWER_ON	–
L55	VDDIN_PWR_BAD_N	VIN_PWR_BAD_N	–
L56	THERM_ALERT_N	SNN_TEMP_ALERT_N	GP108
L57	MCLK05	MCLK05_MCLK_40PIN	GP66
L58	PERIPHERAL_RESET_N	SNN_PERIPHERAL_RESET_N	–
L59	RSVD	SNN_CVM_SYS_RESET_N	–
L60	SYS_RESET_N	SYS_RST_IN_N	–
L61	POWER_BTN_N	POWER_BTN_DEB_N	GP04
L62	CARRIER_POWER_ON	CARRIER_POWER_ON	–
L63	PRSNT1	CVM_PRSNT	–

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