NVIDIA Jetson AGX Orin Developer Kit Carrier Board

Specification

SP-10900-001_v1.1 | June 2023

Document History

SP-10900-001_v1.1

Version	Date	Description of Change
1.0	March 16, 2022	Initial release
1.1	June 8, 2023	• Updated the following to indicate two of the Type A connectors are GEN1 only. > Section 1.2: Carrier Board Feature List. > Chapter 2 introduction. > Section 2.1 USB Ports. • Corrected PCIe Endpoint clock pin name for PCIe connector in Figure 1-1: Jetson AGX Orin Carrier Board Block Diagram • Updated Figure 1-3: Jetson AGX Orin Carrier Board Placement Non-Module Connector Side; added missing RTC back-up connector. • Added note about device usage on Type C connectors in Section 2.1 USB Ports. • Corrected module pin #s for connector pin #s A10/A11 and B10/B11 in Table 2-1: USB 3.2 Type C Connector Pin Descriptions for J40. USB Type C Connector (J40). • Corrected USB 3.2 port #s in Usage/Description Column in Table 2-2: USB 3.2 Type C Connector Pin Descriptions for J39 USB Type C Connector (J39). • Corrected USB 3.2 port #s in Usage/ Description Column in Table 2-3: USB 3.2 Type A Stacked Connector Pin Descriptions for J24 USB Type A Stacked Connector (J24): • Updated DPHY/CPHY and max lengths in Table 3-2 and Table 3-3. • Updated figure title and corrected signal name for pin 13 in Figure 3-5: 40-pin Expansion Header Top View. • Updated the following in Table 3-4: 40-Pin Expansion Header Pin Description > Added GPIO to the list above the table. > Moved note from below the table to above the table related to TXB0108 level tranlators. > Removed highlighting for several pins in SoC GPIO Port # column. • Added note above figure with weight of DevKit in Figure 5-3: Developer Kit Mechanical Dimensions – Top View.

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Chapter 1. Introduction

This specification contains recommendations and guidelines for engineers to follow to create modules for the expansion connectors on the NVIDIA® Jetson™ AGX Orin Developer Kit carrier board as well as understand the capabilities of the other dedicated interface connectors and associated power solutions on the platform.

> **!** CAUTION: ALWAYS CONNECT THE JETSON AGX ORIN SERIES MODULE AND ALL EXTERNAL PERIPHERAL DEVICES BEFORE CONNECTING THE POWER SUPPLY TO THE DEVELOPER KIT.
>
> The Jetson AGX Orin Developer Kit carrier board contains ESD-sensitive parts. Always use appropriate anti-static and grounding techniques when working with the system. Failure to do so can result in ESD discharge to sensitive pins, and irreparably damage your Jetson AGX Orin carrier board. NVIDIA will not replace units that have been damaged due to ESD discharge

The Jetson AGX Orin carrier board connectors are used to access Jetson AGX Orin features and interfaces. This enables a highly flexible and extensible development platform. Go to https://developer.nvidia.com/embedded-computing or contact your NVIDIA representative for access to software updates and the developer SDK that supports the OS image and host development platform that you want to use. The developer SDK includes an OS image that you will load onto your Jetson AGX Orin device, supporting documentation, and code samples to help you get started.

1.1 Jetson AGX Orin Series Feature List

The following is a list of features for the Jetson AGX Orin Series module.

- Applications processor
  - NVIDIA Orin™
- Memory
  - LPDDR5 DRAM
  - eMMC 5.1
- Advanced power management
  - Dynamic voltage and frequency scaling
  - Multiple clock and power domains
  - Thermal transfer plate (TTP) and optional fan or heat sink

1.2 Carrier Board Feature List

The following is a list of features for the carrier board.

- Connection to Jetson AGX Orin
  - 699-pin (11 × 65) board-board connector
- Storage
  - MicroSD Card
  - M.2 Key M connector supporting NVMe
- USB
  - 4× USB 3.2 Type A connectors (2× Gen 1 and 2× Gen 2)
  - 2× USB Type C connectors
- Wired Network
  - MGBE: Up to 10Gb/s to RJ45 connector
- PCI Express
  - Standard PCIe ×16 connector
    - Lower ×8 used for PCIe (Upper ×8 reserved)
- Display
  - VESA® DisplayPort® (DP) output connector
- Camera Expansion Header
  - 120-pin (2 × 60) Board-Board
  - Camera
    - CSI: 16 lanes (6, ×2 or 4, ×4) DPHY or CPHY
    - Camera CLK, I2C and Control
- M.2 Key E Connector
  - PCIe ×1 Lane, USB 2.0
  - I2S, UART, Control
- M.2 Key M Connector
  - PCIe ×4 Lane, Control
- Expansion Header
  - 40-pin (2 × 20) header
  - I2C, SPI, UART, I2S, CAN, D-MIC, PWM, and GPIOs
- UI and Indicators
  - Power, Reset and Force Recovery Buttons
  - Automation Header
    - Power, Reset, Force Recovery, Sleep, Overcurrent, Auto-Power-ON Enable
  - LED: Main 5.0V Supply

- Debug
  - JTAG Connector (2 × 5-pin header)
  - USB Micro B Debug Connector
- Miscellaneous
  - Fan Connector: 5V, PWM, and Tach
- Power
  - 2× USB Type C (either for power input - 19V Adapter included)
  - DC Jack: 7V to 20V (Alternative to Type C)
  - Main 5V Supply: TPS53015
  - Main 3.3V Supply: TPS53015
  - Main 1.8V Buck Supply: MP2384
  - USB Type A VBUS Load Switches: AP22811 (x2)
  - 12V Buck-Boost (PCIe): NCP81599
  - Load Switches/LDOs (SD, DP, and Camera)
- Developer Kit Operating Temperature Range
  - 0 ^{0}C to 35 ^{0}C

Note: All occurrences of USB 3.2 refer to "USB 3.2 Gen 1x1: SuperSpeed USB 5Gbps" and "USB 3.2 Gen 2x1: SuperSpeed USB 10Gbps" only. Also note that Gen 1x1 and Gen 2x1 are referred to simply as Gen 1 and Gen 2 in the document.

1.3 Jetson AGX Orin Carrier Board Block Diagram

Figure 1-1 through Figure 1-3 show the block diagram and various placement views for Jetson AGX Orin and the carrier board.

Figure 1-1. Jetson AGX Orin Carrier Board Block Diagram

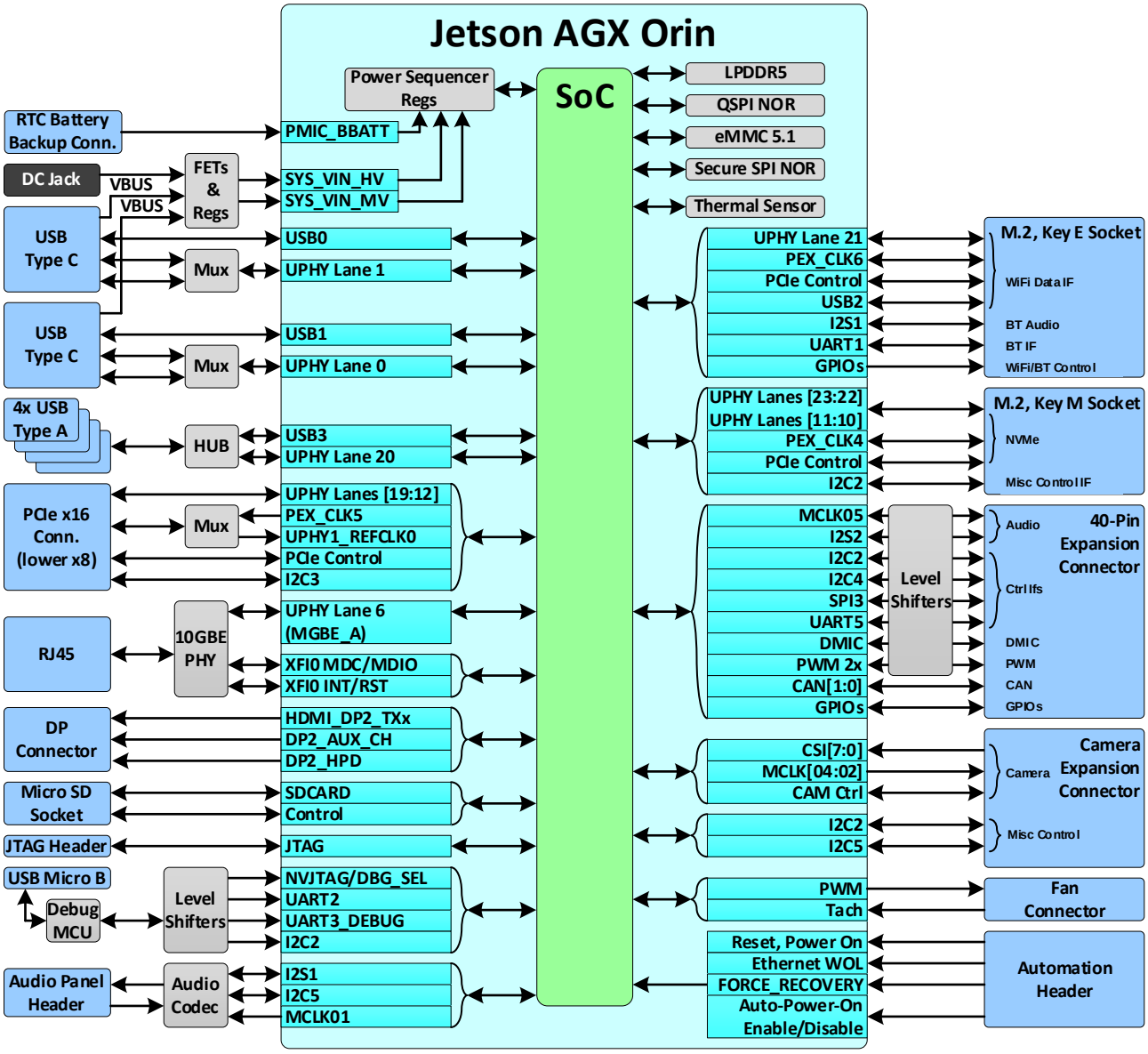
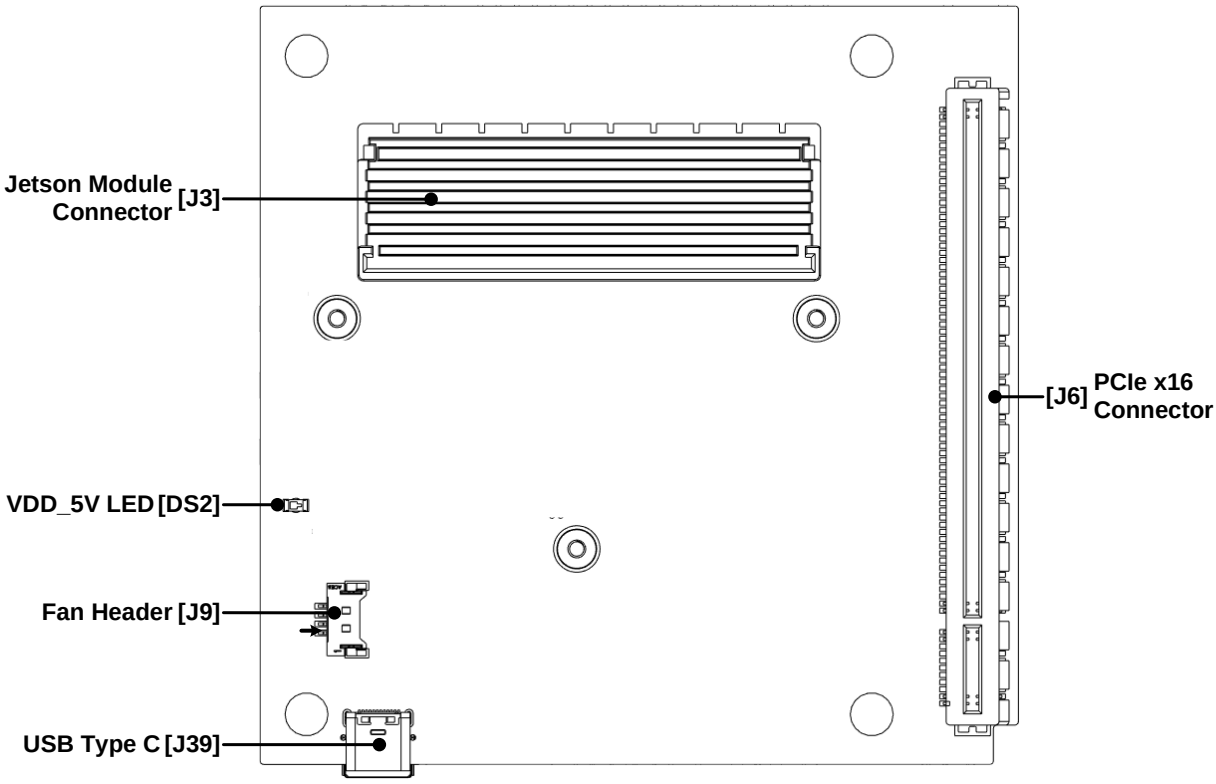
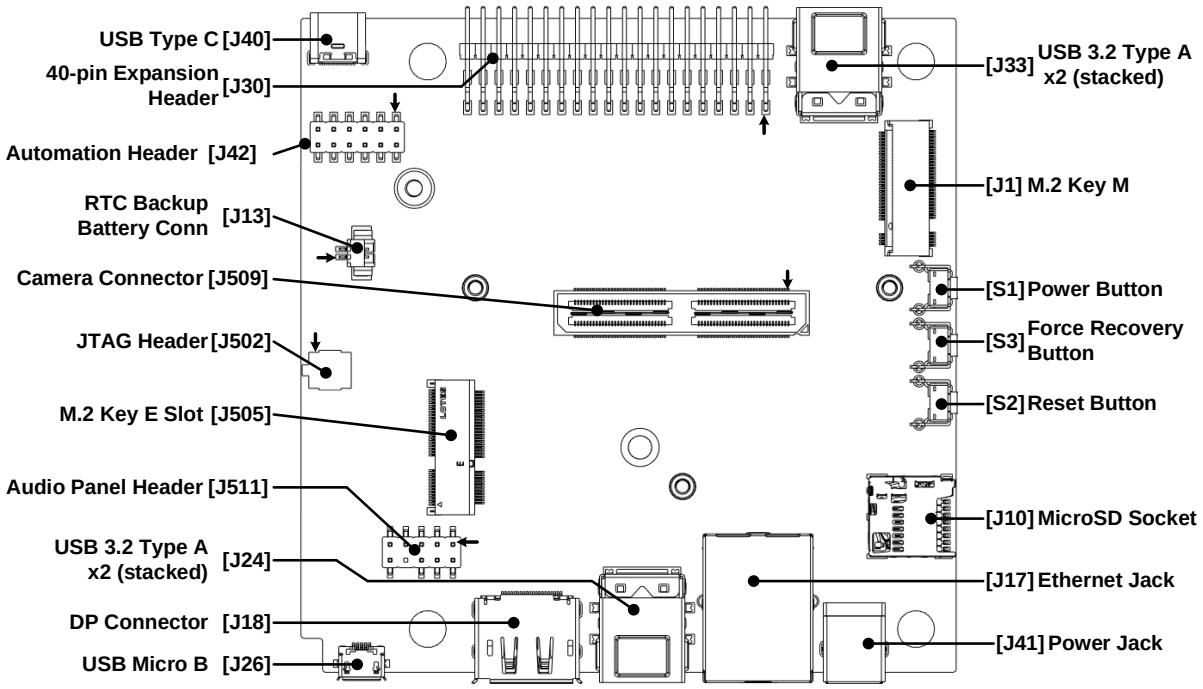


Figure 1-2. Jetson AGX Orin Carrier Board Placement Module Connector Side



J3	Jetson AGX Orin Connector (65x11)	J39	USB Type C Connector #1
J6	PCIe x16 Connector	DS2	VDD_5V LED
J9	Fan Header (4-pin, 1.25mm pitch)		

Figure 1-3. Jetson AGX Orin Carrier Board Placement Non-Module Connector Side



J1	M.2 Key M Slot (75-pin)	J41	Power Jack
J10	MicroSD Socket	J42	Automation Header (2x6, 2.54mm pitch)
J13	RTC Battery Backup Conn. (2-pin, 1.25mm pitch)	J502	JTAG Header (2x5, 1.27 pitch)
J17	RJ45 Ethernet Jack	J505	M.2 Key E Connectivity Slot (75-pin)
J18	DP Connector	J509	Camera Connector (2x60, 0.5mm pitch)
J24	USB 3.2 Type-A Connector (2x Stacked) #1	J511	Audio Panel Header (2x5, 2.54mm pitch)
J26	USB Micro B	S1	Power-on Button
J30	40-Pin Expansion Header (2x20, 2.54mm pitch)	S2	Reset Button
J33	USB 3.2 Type-A Connector (2x Stacked) #2	S3	Force Recovery Button
J40	USB Type C Connector #2		

Chapter 2. Jetson Carrier Board Standard Connectors

The Jetson AGX Orin carrier board provides several standard expansion connectors to support additional functionality beyond what is integrated on the main platform board. This includes the following:

- USB 3.2 Type A: 2× Stacked (4× total. 2× Gen 2 and 2× Gen 1)
- USB Type C: 2×
- USB Micro B (debug)
- RJ45 Connector
- DP Connector
- PCIe ×16 Connector
- Micro SD Card Socket
- M.2, Key E Slot
- M.2, Key M Slot
- Audio Panel Header
- JTAG Header

2.1 USB Ports

The carrier board has the following USB connectors:

- 2× USB Type C Connectors (J39 and J40). Both support USB 3.2 and USB 2.0. J40 supports host and device modes as well as recovery mode. J39 supports host and device modes. VBUS supports up to 5A per Type C connector.
  Note: Only one of the Type C connectors can support Device mode at a time.
- 2× stacked (×2) USB type A connectors (J33 and J24). Each stack has two USB Type A connectors that support host mode for USB 3.2 and USB 2.0. The J24 stack connectors support up to USB 3.2 Gen 2 while the J33 stack support only up to Gen 1. VBUS for each stack of 2× USB Type A connectors supports up to 2A which is shared between the two connectors in the stack.
- Micro B USB connector (J26). Used only for debug purposes.

2.1.1 USB Type C

Table 2-1 and Table 2-2 list the USB 3.2 Type C connector pin descriptions for J40 and J39.

Table 2-1. USB 3.2 Type C Connector Pin Descriptions for J40

Pin #	Connector Pin Name	Associated Module Pin Name (see note 1)	Module Pin #	Usage/Description	Type/Dir
A1	GND_A	–	–	Ground	Ground
A2	TX1_P	UPHY_TX1_P	G23	USB 3.2 #1 Transmit 1 from Mux	Output
A3	TX1_N	UPHY_TX1_N	G22		
A4	–	–	–	USB VBUS_A Power	Power
A5	CC1	–	–	CC 1 from CC Controller	Output
A6	D1_P	USB0_P	F12	USB 2.0 #0 Data 1	Bidir
A7	D1_N	USB0_N	F13		
A8	SBU1	–	–	Unconnected	–
A9	–	–	–	USB VBUS_A Power	Power
A10	RX2_N	UPHY_RX1_N	C22	USB 3.2 #1 Receive 2 from Mux	Input
A11	RX2_P	UPHY_RX1_P	C23		
A12	GND_A	–	–	Ground	Ground
B1	GND_B	–	–	Ground	Ground
B2	TX2_P	UPHY_TX1_P	G23	USB 3.2 #1 Transmit 2 from Mux	Output
B3	TX2_N	UPHY_TX1_N	G22		
B4	–	–	–	USB VBUS_A Power	Power
B5	CC2	–	–	CC 2 from CC Controller	Output
B6	D2_P	USB0_P	F12	USB 2.0 #0 Data 2	Bidir
B7	D2_N	USB0_N	F13		
B8	SBU2	–	–	Unconnected	–
B9	–	–	–	USB VBUS_A Power	Power
B10	RX1_N	UPHY_RX1_N	C22	USB 3.2 #1 Receive 1 from Mux	Input
B11	RX1_P	UPHY_RX1_P	C23		
B12	GND_B	–	–	Ground	Ground

Notes:

1. The module pins for the USB 3.2 ports are not directly connected to the USB connector pins but are routed through a multiplexer.
2. In the Type/Dir column, Output is to USB connectors. Input is from USB connectors. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved/Unused

Table 2-2. USB 3.2 Type C Connector Pin Descriptions for J39

Pin #	Connector Pin Name	Associated Module Pin Name (see note 1)	Module Pin #	Usage/Description	Type/Dir
A1	GND_A	–	–	Ground	Ground
A2	TX1_P	UPHY_TX0_P	J22	USB 3.2 #0 Transmit 1 from Mux	Output
A3	TX1_N	UPHY_TX0_N	J23		
A4	–	–	–	USB VBUS_B Power	Power
A5	CC1	–	–	CC 1 from CC Controller	Output
A6	D1_P	USB1_P	C11	USB 2.0 #0 Data 1	Bidir
A7	D1_N	USB1_N	C10		
A8	SBU1	–	–	Unconnected	–
A9	–	–	–	USB VBUS_B Power	Power
A10	RX2_N	UPHY_RX0_N	A23	USB 3.2 #0 Receive 2 from Mux	Input
A11	RX2_P	UPHY_RX0_P	A22		
A12	GND_A	–	–	Ground	Ground
B1	GND_B	–	–	Ground	Ground
B2	TX2_P	UPHY_TX0_P	J22	USB 3.2 #0 Transmit 2 from Mux	Output
B3	TX2_N	UPHY_TX0_N	J23		
B4	–	–	–	USB VBUS_B Power	Power
B5	CC2	–	–	CC 2 from CC Controller	Output
B6	D2_P	USB1_P	C11	USB 2.0 #0 Data 2	Bidir
B7	D2_N	USB1_N	C10		
B8	SBU2	–	–	Unconnected	–
B9	–	–	–	USB VBUS_B Power	Power
B10	RX1_N	UPHY_RX0_N	A23	USB 3.2 #0 Receive 1 from Mux	Input
B11	RX1_P	UPHY_RX0_P	A22		
B12	GND_B	–	–	Ground	Ground

Notes:

1. The module pins for the USB 3.2 ports are not directly connected to the USB connector pins but are routed through a multiplexer.
2. In the Type/Dir column, Output is to USB connectors. Input is from USB connectors. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved/Unused

2.1.2 USB Type A Stacked Connectors from Hub

Table 2-3 and Table 2-4 list the USB 3.2 Type A stacked connector pin descriptions for J24 and J33.

Table 2-3. USB 3.2 Type A Stacked Connector Pin Descriptions for J24

Pin #	Connector Pin Name (Note 1)	Associated Module Pin Name (Note 2)	Module Pin #	Usage/Description	Type/Dir
USB 3.2 Type A (0)					
1	VBUS	–	–	VBUS Supply	Power
2	DN_0 (DSP2)	USB3_N	G10	USB 2.0 #3 Data (stack connector 2)	Bidir
3	DP_0 (DSP2)	USB3_P	G11		
4	GND	–	–	Ground	Ground
5	RX_N_0 (DSP2)	UPHY_RX20_N	C35	USB 3.2 (SoC Port 2) Receive (stack connector 2)	Input
6	RX_P_0 (DSP2)	UPHY_RX20_P	C34		
7	GND	–	–	Ground	Ground
8	TX_N_0 (DSP2)	UPHY_TX20_N	K33	USB 3.2 (SoC Port 2) Transmit (stack connector 2)	Output
9	TX_P_0 (DSP2)	UPHY_TX20_P	K32		
USB 3.2 Type A (1)					
10	VBUS	–	–	VBUS Supply	Power
11	DN_1 (DSP1)	USB3_N	G10	USB 2.0 #3 Data (stack connector 1)	Bidir
12	DP_1 (DSP1)	USB3_P	G11		
13	GND	–	–	Ground	Ground
14	RX_N_1 (DSP1)	UPHY_RX20_N	C35	USB 3.2 (SoC Port 2) Receive (stack connector 1)	Input
15	RX_P_1 (DSP1)	UPHY_RX20_P	C34		
16	GND	–	–	Ground	Ground
17	TX_N_1 (DSP1)	UPHY_TX20_N	K33	USB 3.2 (SoC Port 2) Transmit (stack connector 1)	Output
18	TX_P_1 (DSP1)	UPHY_TX20_P	K32		

Notes:
1. These signals are from the Hub.
2. These are from the Jetson AGX Orin to the Hub.
3. In the Type/Dir column, Output is to USB connectors. Input is from USB connectors. Bidir is for bidirectional signals.

Legend: Ground | Power

Table 2-4. USB 3.2 Type A Stacked Connector Pin Descriptions for J33

Pin #	Connector Pin Name (Note 1)	Associated Module Pin Name (Note 2)	Module Pin #	Usage/Description	Type/Dir
USB 3.2 Type A (0)					
1	VBUS	–	–	VBUS Supply	Power
2	DN_0 (DSP4)	USB3_N	G10	USB 2.0 #3 Data (stack connector 4)	Bidir
3	DP_0 (DSP4)	USB3_P	G11		
4	GND	–	–	Ground	Ground
5	RX_N_0 (DSP4)	UPHY_RX20_N	C35	USB 3.2 (SoC Port 0) Receive (stack connector 4)	Input
6	RX_P_0 (DSP4)	UPHY_RX20_P	C34		
7	GND	–	–	Ground	Ground
8	TX_N_0 (DSP4)	UPHY_TX20_N	K33	USB 3.2 (SoC Port 0) Transmit (stack connector 4)	Output
9	TX_P_0 (DSP4)	UPHY_TX20_P	K32		
USB 3.2 Type A (1)					
10	VBUS	–	–	VBUS Supply	Power
11	DN_1 (DSP3)	USB3_N	G10	USB 2.0 #3 Data (stack connector 3)	Bidir
12	DP_1 (DSP3)	USB3_P	G11		
13	GND	–	–	Ground	Ground
14	RX_N_1 (DSP3)	UPHY_RX0_N	A23	USB 3.2 (SoC Port 0) Receive (stack connector 3)	Input
15	RX_P_1 (DSP3)	UPHY_RX0_P	A22		
16	GND	–	–	Ground	Ground
17	TX_N_1 (DSP3)	UPHY_TX0_N	J23	USB 3.2 (SoC Port 0) Transmit (stack connector 3)	Output
18	TX_P_1 (DSP3)	UPHY_TX0_P	J22		

Notes:
1. These signals are from the Hub.
2. These are from the Jetson AGX Orin to the Hub.
3. In the Type/Dir column, Output is to USB connectors. Input is from USB connectors. Bidir is for bidirectional signals.

Legend	Ground	Power

2.1.3 USB Micro B

A USB Micro B connector is provided for debug purposes only. The connector USB 2.0 interface comes from a debug MCU. It takes in the following interfaces and control pins that can be used for debug and development:

- UART3_TX/RX_DEBUG
- UART2_TX/RX

Table 2-5. USB Micro B Debug Connector Pin Descriptions for J26

Pin #	Connector Pin Name	Associated Module Pin Name	Module Pin #	Usage/Description	Type/Dir
1	VBUS	–	–	VBUS Supply	Power
2	DN	–	–	USB 2.0 Data (From Debug MCU)	Bidir
3	DP	–	–		
4	ID	–	–	No Connect	–
5	GND	–	–	Ground	Ground

Note: In the Type/Dir column, Output is to USB connectors. Input is from USB connectors. Bidir is for bidirectional signals.

Legend | Ground | Power

2.2 Multi-Gigabit Ethernet Connector

The carrier board implements an RJ45 connector (J17) with built-in magnetics to support Multi Gigabit Ethernet (MBGE). Data rates supported include 1 Gb, 2.5 Gb, 5 Gb, and 10 Gb.

Table 2-6. MGBE RJ45 Connector Pin Description

Pin #	Connector Pin Name	Associated Module Pin Name (Note 1)	Module Pin #	Usage/Description	Type/Dir
1	TRCT2	–	–	Center tap 2	–
2	TRD2-	UPHY_TX6_N UPHY_RX6_N	K16 B17	MGBE PHY B	Bidir
3	TRD2+	UPHY_TX6_P UPHY_RX6_P	K17 B16		
4	TRD3+	UPHY_TX6_P UPHY_RX6_P	K17 B16	MGBE PHY C	Bidir
5	TRD3-	UPHY_TX6_N UPHY_RX6_N	K16 B17		
6	TRCT3	–	–	Center tap 3	–
7	TRCT1	–	–	Center tap 1	–
8	TRD1+	UPHY_TX6_P UPHY_RX6_P	K17 B16	MGBE PHY A	Bidir
9	TRD1-	UPHY_TX6_N UPHY_RX6_N	K16 B17		
10	TRD4-	UPHY_TX6_N UPHY_RX6_N	K16 B17	MGBE PHY D	Bidir
11	TRD4+	UPHY_TX6_P UPHY_RX6_P	K17 B16		
12	TRCT4	–	–	Center tap 4	–
L1	GRN- (Left)	–	–	Left green LED cathode	Input
L2	COM+(Left)	–	–	Left LED common (anode)	Power
L3	YEL-(Left)	–	–	Left green LED cathode	Input
L4	GRN- (Right)	–	–	Right green LED cathode	Input

Pin #	Connector Pin Name	Associated Module Pin Name (Note 1)	Module Pin #	Usage/Description	Type/Dir
L5	COM+(Right)	–	–	Right LED common (anode)	Power
L6	YEL-(Right)	–	–	Right green LED cathode	Input

Notes:

1. The module pins for the MBGE port are not directly connected to the RJ45 connector pins but are routed through a an MBGE PHY.
2. In the Type/Dir column, Output is to RJ45 connector. Input is from RG45 connector. Bidir is for bidirectional signals.

2.3 DisplayPort Connector

A standard DisplayPort (DP) connector (J18) is supported. This connector can support HDMI™ with the correct dongle.

Table 2-7. DisplayPort Connector Pin Description

Pin #	Connector Pin Name	Associated Module Pin Name	Module Pin #	Usage/Description	Type/Dir
1	LANE_0P	HDMI_DP2_TX0_P	D51	DP Lane 0+	Output
2	GND	–	–	Ground	Ground
3	LANE_0N	HDMI_DP2_TX0_N	D52	DP Lane 0–	Output
4	LANE_1P	HDMI_DP2_TX1_P	B51	DP Lane 1+	Output
5	GND	–	–	Ground	Ground
6	LANE_1N	HDMI_DP2_TX1_N	B52	DP Lane 1–	Output
7	LANE_2P	HDMI_DP2_TX2_P	A51	DP Lane 2+	Output
8	GND	–	–	Ground	Ground
9	LANE_2N	HDMI_DP2_TX2_N	A50	DP Lane 2–	Output
10	LANE_3P	HDMI_DP2_TX3_P	C51	DP Lane 3+	Output
11	GND	–	–	Ground	Ground
12	LANE_3N	HDMI_DP2_TX3_N	C50	DP Lane 3–	Output
13	MODE	–	–	MODE: Selects between DP and TMDS (DVI/HDMI) signaling.	Unused
14	CEC	HDMI_CEC	J50	Consumer Electronics Control	Bidir
15	AUXP	DP2_AUX_CH_P	G53	DisplayPort Auxiliary Channel 0+	Bidir
16	GND	–	–	Ground	Ground
17	AUXN	DP2_AUX_CH_N	G54	DisplayPort Auxiliary Channel 0-	Bidir
18	HPD	DP2_HPD	K50	HDMI Hot Plug Detect	Input
19	PWR_RET	–	–	Power Return (Ground)	Ground
20	PWR	–	–	+3.3V	Power

Note: In the Type/Dir column, Output is to DP connector. Input is from DP connector. Bidir is for bidirectional signals.

Legend	Ground	Power

2.4 PCIe x16 Connector

The Jetson carrier board includes a standard PCIe ×16 connector (J6). The upper ×8 portion supports up to 8 PCIe lanes which are assigned to PCIe controller #5. This connector can support PCIe Endpoint or Root Port cards.

The upper ×8 portion of the connector is not used. Connections to those pins are for internal testing only.

Table 2-8. PCIe x16 Connector Lower x8 Portion Pin Description

Pin #	Connector Pin Name	Assoc. Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level
A1	PRSNT1*	–	–	Tied to GND	–	–
A2, A3	+12V	–	–	12V Supply	PWR	+12V
A4	GND	–	–	Ground	GND	–
A5, A6, A7, A8	NC	–	–	Unused	–	–
A9, A10	+3.3	–	–	3.3V Supply	PWR	+3.3
A11	PERST*	PEX_L5_RST_N	H10	PCIe Reset		3.3V, Open Drain
A12	GND	–	–	Ground	GND	–
A13	REFCLK	PEX_CLK5_P / UPHY_REFCLK0_P	F24 E31	PCIe #5 Clock output or UPHY Reference clock #0 input (via mux)	Output Input	PCIe
A14	REFCLK*	PEX_CLK5_N / UPHY_REFCLK0_N	F25 E30			
A15	GND	–	–	Ground	GND	–
A16	PERP0	UPHY_RX12_P	D24	PCIe Receive (C5) Lane 0	Input	PCIe
A17	PERN0*	UPHY_RX12_N	D25			
A18	GND	–	–	Ground	GND	–
A19	RSVD	–	–	Unused	–	–
A20	GND	–	–	Ground	GND	–
A21	PERP1	UPHY_RX13_P	B25	PCIe Receive (C5) Lane 1	Input	PCIe
A22	PERN1*	UPHY_RX13_N	B24			
A23, A24	GND	–	–	Ground	GND	–
A25	PERP2	UPHY_RX14_P	C27	PCIe Receive (C5) Lane 2	Input	PCIe
A26	PERN2*	UPHY_RX14_N	C26			
A27, A28	GND	–	–	Ground	GND	–
A29	PERP3	UPHY_RX15_P	A26	PCIe Receive (C5) Lane 3	Input	PCIe
A30	PERN3*	UPHY_RX15_N	A27			
A31	GND	–	–	Ground	GND	–
A32, A33	RSVD	–	–	Unused	–	–
A34	GND	–	–	Ground	GND	–
A35	PERP4	UPHY_RX16_P	D28	PCIe Receive (C5) Lane 4	Input	PCIe
A36	PERN4*	UPHY_RX16_N	D29			
A37, A38	GND	–	–	Ground	GND	–
A39	PERP5	UPHY_RX17_P	B29	PCIe Receive (C5) Lane 5	Input	PCIe
A40	PERN5*	UPHY_RX17_N	B28			
A41, A42	GND	–	–	Ground	GND	–

Pin #	Connector Pin Name	Assoc. Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level
A43	PERP6	UPHY_RX18_P	C31	PCIe Receive (C5) Lane 6	Input	PCIe
A44	PERN6*	UPHY_RX18_N	C30			
A45, A46	GND	–	–	Ground	GND	–
A47	PERP7	UPHY_RX19_P	A30	PCIe Receive (C5) Lane 7	Input	PCIe
A48	PERN7*	UPHY_RX19_N	A31			
A49	GND	–	–	Ground	GND	–
B1, B1, B3	+12V	–	–	12V Supply	PWR	+12V
B4	GND	–	–	Ground	GND	–
B5	SMCLK	I2C3_CLK	F53	I2C Misc.	Bidir	3.3V, open-drain
B6	SMDAT	I2C3_DAT	E53		Bidir	
B7	GND	–	–	Ground	GND	–
B8	+3.3	–	–	3.3V Supply	PWR	+3.3
B9	TRST* JTAG1	–	–	Unused	–	–
B10	+3.3AUX	–	–	3.3V Aux Supply	PWR	+3.3AUX
B11	WAKE*	PCIE_WAKE_N	A8	PCIe Wake	Output	3.3V, Open Drain
B12	CLKREQ*	PEX_L5_CLKREQ_N	C8	PCIe Clock Request	Output	3.3V, Open Drain
B13	GND	–	–	Ground	GND	–
B14	PETP0	UPHY_TX12_P	H24	PCIe Transmit (C5) Lane 0	Output	PCIe
B15	PETN0	UPHY_TX12_N	H25			
B16	GND	–	–	Ground	GND	–
B17	PRSNT2*	GPIO31	H60	PCIe Present	Output	
B18	GND	–	–	Ground	GND	–
B19	PETP1	UPHY_TX13_P	K25	PCIe Transmit (C5) Lane 1	Output	PCIe
B20	PETN1*	UPHY_TX13_N	K24			
B21, B22	GND	–	–	Ground	GND	–
B23	PETP2	UPHY_TX14_P	G27	PCIe Transmit (C5) Lane 2	Output	PCIe
B24	PETN2*	UPHY_TX14_N	G26			
B25, B26	GND	–	–	Ground	GND	–
B27	PETP3	UPHY_TX15_P	J26	PCIe Transmit (C5) Lane 3	Output	PCIe
B28	PETN3*	UPHY_TX15_N	J27			
B29	GND	–	–	Ground	GND	–
B30	PWRBRK	–	–	Unused	–	
B31	PRSNT2*	GPIO31	H60	PCIe Present	Output	1.8V (3.3V tolerant)
B32	GND	–	–	Ground	GND	–
B33	PETP4	UPHY_TX16_P	H28	PCIe Transmit (C5) Lane 4	Output	PCIe
B34	PETN4*	UPHY_TX16_N	H29			
B35, B36	GND	–	–	Ground	GND	–
B37	PETP5	UPHY_TX17_P	K29	PCIe Transmit (C5) Lane 5	Output	PCIe
B38	PETN5*	UPHY_TX17_N	K28			
B39, B40	GND	–	–	Ground	GND	–
B41	PETP6	UPHY_TX18_P	G31	PCIe Transmit (C5) Lane 6	Output	PCIe
B42	PETN6*	UPHY_TX18_N	G30			
B43, B44	GND	–	–	Ground	GND	–
B45	PETP7	UPHY_TX19_P	J30	PCIe Transmit (C5) Lane 7	Output	PCIe

Pin #	Connector Pin Name	Assoc. Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level
B46	PETN7*	UPHY_TX19_N	J31			
B47	GND	–	–	Ground	GND	–
B48	PRSNT2*	GPIO_31	H60	PCIe Present	Output	1.8V (3.3V tolerant)
B49	GND	–	–	Ground	GND	–

Note: In the Type/Dir column, Output is to PCIe connector. Input is from PCIe connector. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved/Unused

2.4.1 Maximum PCIe Card Routing Delays

The routing on the developer kit carrier board meets the requirements in the *NVIDIA DRIVE Orin Module Design Guide* for routing to a PCIe and M.2 connector. Therefore, the maximum allowed routing on the PCIe adapter card is what is allowed by the PCIe specification. The design guide provides an insertion loss of 9.6 dB for Gen3 and 8.0 dB for Gen4. Using the mid-loss PCB technology loss numbers from the design guide, that translates to the values listed in Table 2-9.

Table 2-9. PCIe Card Maximum Trace Delays

PCIe	Max Trace Length Allowed on PCIe Card
Gen3	220.0 mm
Gen4	150.5 mm

2.5 Micro SD Card Socket

A Micro SD Card Socket (J10) is implemented on the developer kit carrier board. The SD card interface supports up to SDR104 mode (UHS-1).

Table 2-10. SD Card Connector Pin Description

Pin #	Connector Pin Name	Associated Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level
1	DAT2	SDCARD_D2	A4	SD Card Data #2	Bidir	1.8V/3.3V
2	CD/DAT3	SDCARD_D3	D6	SD Card Data #3	Bidir	1.8V/3.3V
3	CMD	SDCARD_CMD	A5	SD Card Command	Bidir	1.8V/3.3V
4	VDD	–	–	3.3V Power Rail	PWR	3.3V
5	CLK	SDCARD_CLK	B6	SD Card Clock	Output	1.8V/3.3V
6	VSS	–	–	Ground	GND	
7	DAT0	SDCARD_D0	E8	SD Card Data #0	Bidir	1.8V/3.3V
8	DAT1	SDCARD_D1	F8	SD Card Data #1	Bidir	1.8V/3.3V
9	GND	–	–	Ground	GND	
10						

Pin #	Connector Pin Name	Associated Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level
11						
12						
13	C_DETECT1	GPIO02	L6	SD Card, Card Detect	Input	1.8V
14	C_DETECT2	–	–	Common – tied to Ground	–	
	–	GPIO21	B58	SD Card load switch enable	Output	3.3V

Note: In the Type/Dir column, Output is to SD Card socket. Input is from SD Card socket. Bidir is for bidirectional signals.

Legend	Ground	Power

2.6 M.2 Key E Expansion Slot

The Jetson carrier board includes an M.2, Key E slot (J505). This includes interface options for WLAN/BT including PCIe (×1), USB 2.0, UART, and I2S.

Table 2-11. M.2 Key E Expansion Slot Pin Description

Pin #	Connector Pin Name	Assoc. Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level
Odd Pins						
1	GND	–	–	Ground	GND	–
3	USB_DP	USB2_P	A10	USB 2.0 #2	Bidir	USB
5	USB_DM	USB2_N	A11			
7	GND	–	–	Ground	GND	–
9,11,13,15,17, 19,21,23	NC	–	–	Unused	–	–
25, 27, 29, 31	Key	–	–	–	–	–
33	GND	–	–	Ground	GND	–
35	AP_PETP0	UPHY_TX21_P	G35	PCIe Transmit (C0)	Output	PCIe
37	AP_PETN0	UPHY_TX21_N	G34			
39	GND	–	–	Ground	GND	–
41	AP_PERP0	UPHY_RX21_P	B33	PCIe Receive (C1)	Input	PCIe
43	AP_PERN0	UPHY_RX21_N	B32			
45	GND	–	–	Ground	GND	–
47	REFCLKP0	PEX_CLK6_P	D49	PCIe Reference Clock (C1)	Output	PCIe
49	REFCLKN0	PEX_CLK6_N	D48			
51	GND	–	–	Ground	GND	–
53	CLKREQ0#	PEX_C7_CLKREQ_N	B37	PCIe Clock Request (C1)	Bidir	3.3V
55	PEWAKE0#	GPIO23	G55	PCIe Wake (see note 2)	Output	3.3V
57	GND	–	–	Ground	GND	–
59	AP_RESERVED/PETP 1	SPI1_MOSI	D55	SAR TOUT	Output	
61	NC	–	–	Unused	–	–
63	GND	–	–	Ground	GND	–

Pin #	Connector Pin Name	Assoc. Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level
Odd Pins						
65, 67	NC	–	–	Unused	–	–
69	GND	–	–	Ground	GND	–
71, 73	NC	–	–	Unused	–	–
75	GND	–	–	Ground	GND	–
Even Pins						
2, 4	3P3V	–	–	3.3V Supply	PWR	–
6	LED1#	–	–	Unused	–	–
8	PCM_CLK/12S SCK	I2S3_CLK	C59	I2S Clock	Bidir	
10	PCM_SYNC/12S WS	I2S3_FS	C60	I2S Frame/Word Select	Bidir	
12	AP_PCM_IN/12S SD_IN	I2S3_SDIN	J59	I2S Data In	Input	
14	AP_PCM_OUT/12S SD_OUT	I2S3_SDOUT	K59	I2S Data Out	Output	
16	LED2#	–	–	Unused	–	–
18	GND	–	–	Ground	GND	–
20	UART_WAKE#	GPIO32	J55	BT Wake SoC Primary	Output	
22	AP_UART_RXD	UART5_RX	H58	UART Receive	Input	
24, 26,.28,.30	Key	–	–	–	–	–
32	AP_UART_TXD	UART5_TX	J58	UART Transmit	Output	
34	AP_UART_CTS	UART5_CTS	H57	UART Clear to Send	Input	
36	AP_UART_RTS	UART5_RTS	K58	UART Ready to Send	Output	
38,40,42,44, 46,48	NC	–	–	Unused	–	–
50	SUSCLK_32KHZ	–	–	Suspend Clock	Output	
52	PERST0#	PEX_C7_RST_N	B36	PCIe Reset (C1)	Output	
54	W_DISABLE2#	DP0_AUX_CH_P	F52	WLAN Reset	Output	
56	W_DISABLE1#	GPIO05	A59	WLAN Disable	Output	
58, 60	NC	–	–	Unused	–	–
62	ALERT#	GPIO32	J55	Alert to SoC	Input	
64, 66, 68, 70	NC	–	–	Unused	–	–
72, 74	3P3V	–	–	3.3V Supply	PWR	–

Notes:

1. Series resistors R842 & R843 are unstuffed by default disconnecting the I2C signals from the M.2 Key E connector.
2. GPIO23 pass through 1.8V-3.3V level shifter before being routed to the M.2 connector pin.
3. In the Type/Dir column, Output is to M.2 connector. Input is from M.2 connector. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved/Unused

2.6.1 Maximum M.2 Key E Card Routing Delays

The routing on the developer kit carrier board meets the requirements in the *NVIDIA DRIVE Orin Module Design Guide* for routing to an M.2 connector. Therefore, the maximum allowed routing on the M.2 adapter card is based on the insertion loss allocated for the card which is 9.6 dB for Gen3. Using the mid-loss PCB technology loss numbers from the design guide, that translates to the values listed in Table 2-12.

Table 2-12. M.2 Key E Card Maximum Trace Delays

PCIe	Max Trace Delay Allowed on M.2 Card
Gen3	311 mm (average of Microstrip and Stripline guidelines)

2.7 M.2 Key M Expansion Slot

The carrier board includes an M.2, Key M slot expansion slot (J1). This includes four UPHY lanes that can be configured for PCIe (×4). The connector used is a Wieson Technologies AC6155-0011-004-HH part.

Table 2-13. M.2 Key M Expansion Slot Pin Description

Pin #	Connector Pin Name	Assoc. Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level
Odd Pins						
1,3	GND	–	–	Ground	GND	–
5	PER3_N	UPHY_RX22_N	D32	PCIe Receive Lane 3 (C4)	Input	PCIe
7	PER3_P	UPHY_RX22_P	D33			
9	GND	–	–	Ground	GND	–
11	PET3_N	UPHY_TX22_N	J34	PCIe Transmit Lane 3 (C4)	Output	PCIe
13	PET3_P	UPHY_TX22_P	J35			
15	GND	–	–	Ground	GND	–
17	PER2_N	UPHY_RX23_N	A35	PCIe Receive Lane 2 (C4)	Input	PCIe
19	PER2_P	UPHY_RX23_P	A34			
21	GND	–	–	Ground	GND	–
23	PET2_N	UPHY_TX23_N	H33	PCIe Transmit Lane 2 (C4)	Output	PCIe
25	PET2_P	UPHY_TX23_P	H32			
27	GND	–	–	Ground	GND	–
29	PER1_N	UPHY_RX10_N	B13	PCIe Receive Lane 1 (C4)	Input	PCIe
31	PER1_P	UPHY_RX10_P	B12			
33	GND	–	–	Ground	GND	–
35	PET1_N	UPHY_TX10_N	K12	PCIe Transmit Lane 1 (C4)	Output	PCIe
37	PET1_P	UPHY_TX10_P	K13			
39	GND	–	–	Ground	GND	–
41	PER0_N	UPHY_RX11_N	D13	PCIe Receive Lane 0 (C4)	Input	PCIe
43	PER0_P	UPHY_RX11_P	D12			

Pin #	Connector Pin Name	Assoc. Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level
Odd Pins						
45	GND	–	–	Ground	GND	–
47	PET0_N	UPHY_TX11_N	H13	PCIe Transmit Lane 0 (C4)	Output	PCIe
49	PET0_P	UPHY_TX11_P	H12			
51	GND	–	–	Ground	GND	–
53	REFCLK_N	PEX_CLK4_N	E22	PCIe Reference Clock (C4)	Output	PCIe
55	REFCLK_P	PEX_CLK4_P	E23			
57	GND	–	–	Ground	GND	–
59, 61, 63, 65	Key	–	–	–	–	–
67, 69	N/C	–	–	Unused	–	–
71, 73, 75	GND	–	–	Ground	GND	–
Even Pins						
2, 4	3V3	–	–	3.3V Supply	PWR	3.3V
6, 8, 10	N/C	–	–	Unused	–	–
12,14,16,18	3V3	–	–	3.3V Supply	PWR	3.3V
20,24,26,28,30, 32,34,36,38	N/C	–	–	Unused	–	–
40	SMB_CLK	I2C2_CLK	J61	I2C 2 Clock (see note 1)	Bidir	1.8V (3.3V tolerant)
42	SMB_DATA	I2C2_DAT	K61	I2C 2 Data (see note 1)	Bidir	
44	ALERT*	GPIO34	A55	M.2 Key M Alert	Output	1.8V
46, 48	N/C	–		Unused	–	–
50	PERST#	PEX_C4_RST_N	J9	PCIe C4 Reset	Output	3.3V
52	CLKREQ#	PEX_C4_CLKREQ_N	G8	PCIe C4 Clock Request	Bidir	3.3V
54	PEWAKE#	PCIE_WAKE_N	A8	PCIe Wake	Input	3.3V
56	N/C	RSVD	–	RSVD	–	–
58	N/C	RSVD	–	RSVD	–	–
60,62,64,66	Key	–	–	–	–	–
68	SUSCLK	–	–	Suspend Clock	Output	3.3V
70,72,74	3V3	–	–	3.3V Supply	PWR	3.3V

Notes:
1. Series resistors R840 and R841 are unstuffed by default disconnecting the I2C signals from the M.2 Key M connector.
2. In the Type/Dir column, Output is to M.2 connector. Input is from M.2 connector. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved/Unused

2.7.1 Maximum M.2 Key M Card Routing Delays

The routing on the developer kit carrier board meets the requirements in the *NVIDIA DRIVE Orin Module Design Guide* for routing to an M.2 connector. Therefore, the maximum allowed routing on the M.2 adapter card is based on the insertion loss allocated for the card which is 9.6 dB for Gen3 or 8.0 dB for Gen4. Using the mid-loss PCB technology loss numbers from the design guide, that translates to the values listed in the following table.

Table 2-14. M.2 Key M Maximum Trace Delays PCIe to Gen4

PCIe	Max Trace Delay Allowed on M.2 Card
Gen3	321 mm (average of Microstrip and Stripline guidelines)
Gen4	189 mm (average of Microstrip and Stripline guidelines)

2.8 Audio Panel Header

The Jetson carrier board includes a 10-pin (2 × 5, 2.54 mm pitch) audio panel header (J511). This can be used to connect to a standard PC audio panel to support connections to microphone, line-in, headphones, powered speakers, and so on.

Table 2-15. Audio Panel Header Pin Description

Pin #	Connector (Codec) Pin Name	Associated Module Pin Name	Module Pin #	Usage/Description	Type/Dir
1	(IN1P)	–	–	Microphone #1 input	Input
2	AGND	–	–	Ground	GND
3	(IN2P)	–	–	Microphone #2 input	Input
4	(LRCK2/GPIO4/PDM_SDA)	–	–	Presence – detects if audio dongle is connected to header.	Input
5	(HPO_R)	–	–	Headphone output right channel	Output
6	(MIC_IN_DET)	–	–	Jack/Microphone detect pin	Input
7	SENSE_SEND	–	–	Pulled to analog GND	NA
8	Key				
9	(HPO_L)	–	–	Headphone output left channel	Output
10	(BCLK2/GPIO3/PDM_SCL)	–	–	Headphone or jack detection	Input
–	–	AUDIO_MCLK	H9	Audio master clock	Output
–	–	I2S1_CLK	L14	I2S #1 clock	Output
–	–	I2S1_FS	D8	I2S #1 field select	Bidir
–	–	I2S1_SDOUT	C7	I2S #1 data output	Output
–	–	I2S1_SDIN	H8	I2S #1 data input	Input
–	–	GPIO11	B8	Audio interrupt	Output
–	–	I2C5_CLK	A53	I2C #5 clock	Bidir
–	–	I2C5_DAT	C53	I2C #5 data	Bidir

Notes: In the Type/Dir column, Output is to Audio Header. Input is from Audio Header. Bidir is for bidirectional signals.

Legend | Ground | Power

2.9 JTAG Header

The Jetson carrier board has a 10-pin (2 × 5, 1.27 mm pitch) JTAG header (J502).

Table 2-16. JTAG Header Description

Pin #	Connector Pin Name	Associated Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level
1	PWR	–	–	Main 1.8V Supply	Power	1.8V
2	TMS	JTAG_TMS	E58	JTAG Test Mode Select	Input	1.8V
3	GND	–	–	Ground	Ground	–
4	TCK	JTAG_TCK	A60	JTAG Test Clock	Input	1.8V
5	GND	–	–	Ground	Ground	–
6	TDO	JTAG_TDO	D58	JTAG Test Data Out	Output	1.8V
7	GND	–	–	Ground	Ground	–
8	TDI	JTAG_TDI	B60	JTAG Test Data In	Input	1.8V
9	GND	–	–	Ground	Ground	–
10	RST	SYS_RESET_N	L60	Main carrier board reset	Input	1.8V

Note: In the Type/Dir column, Output is to Audio Header. Input is from Audio Header. Bidir is for bidirectional signals.

Legend | Ground | Power |

Chapter 3. Carrier Board Custom Connectors

The Jetson carrier board supports several custom expansion headers:

- Jetson AGX Orin Connector, 65 × 11
- Camera Expansion Header, 2 × 60, 0.5 mm pitch
- Expansion Header, 2 × 20, 2.54 mm pitch
- Automation Header, 2 × 4, 2.54 mm pitch
- Fan Header, 4-pin, 1.25 mm pitch
- DC Power Jack
- RTC Backup Battery Connector, 4-pin, 1.25mm pitch

The routing guidelines for the interfaces supported on the expansion connectors can be found in the *Jetson AGX Orin Product Design Guide*. Those guidelines cover the PCB routing from the Jetson AGX Orin to the peripheral device or actual device connector. When designing modules for one of the Jetson AGX Orin expansion connectors, the routing on the carrier board must be accounted for. Tables are provided for the critical interfaces that provide the PCB delays on the carrier board. These delays are subtracted from the delays allowed in the *Jetson AGX Orin Product Design Guide* routing guidelines. The tables also include the max trace guidelines and remaining max trace delay allowed on the peripheral modules. See the *Jetson AGX Orin Product Design Guide* for other requirements (Impedance, trace spacing, skews between signals, and so on).

3.1 Module Connector

The carrier board interfaces to Jetson AGX Orin using a 699-pin (65 × 11) connector (J3). The part number for the connector used on the carrier board can be found in the Jetson AGX Orin Supported Component List (SCL) document. This interfaces with the module. See the *Jetson AGX Orin Data Sheet* for the connector used on the module. The connector pinout can be found in the *Jetson AGX Orin Product Design Guide*.

3.2 Camera Expansion Connector

The Jetson AGX Orin carrier board includes a 120-pin (2 × 60, 0.5 mm pitch) camera expansion connector (J509). The connector used on the carrier board is a Samtec QSH-060-01-H-D-A. The mating connector is a Samtec QTH-060-0x-H-D-A (x is for the height).

The expansion connector includes interface options for multiple CSI DPHY or CPHY cameras. Refer to the *Jetson AGX Orin Camera Module Hardware Design Guide* for more information.

- CSI up to 4 × 4 lane or 6 × 2 lane
- CAM_I2C, Clock and Control GPIOs for the cameras
- I2C (2x in addition to CAM_I2C)

Table 3-1. Camera Expansion Connector Pin Description

Pin #	Assoc. Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level
1	CSI0_D0_P	E42	CSI 0 Data 0	Input	MIPI DPHY/CPHY
3	CSI0_D0_N	E41			
5	–	–	Ground	Ground	–
7	CSI0_CLK_P	F43	CSI 0 Clock	Input	MIPI DPHY/CPHY
9	CSI0_CLK_N	F42			
11	–	–	Ground	Ground	–
13	CSI0_D1_P	E39	CSI 0 Data 1	Input	MIPI DPHY/CPHY
15	CSI0_D1_N	E38			
17	–	–	Ground	Ground	–
19	CSI2_D0_P	A41	CSI 2 Data 0	Input	MIPI DPHY/CPHY
21	CSI2_D0_N	A42			
23	–	–	Ground	Ground	–
25	CSI2_CLK_P	B43	CSI 2 Clock	Input	MIPI DPHY/CPHY
27	CSI2_CLK_N	B42			
29	–	–	Ground	Ground	–
31	CSI2_D1_P	C42	CSI 2 Data 1	Input	MIPI DPHY/CPHY
33	CSI2_D1_N	C41			
35	–	–	Ground	Ground	–
37	CSI4_D0_P	G48	CSI 4 Data 0	Input	MIPI DPHY/CPHY
39	CSI4_D0_N	G47			
41	–	–	Ground	Ground	–
43	CSI4_CLK_P	F48	CSI 4 Clock	Input	MIPI DPHY/CPHY
45	CSI4_CLK_N	F47			
47	–	–	Ground	Ground	–
49	CSI4_D1_P	E47	CSI 4 Data 1	Input	MIPI DPHY/CPHY
51	CSI4_D1_N	E48			
53	–	–	Ground	Ground	–

Pin #	Assoc. Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level
55 57	–	–	DVDD_CAM_LV. Reserved for Low Voltage Digital Supply	(Power)	–
59	CSI5_D0_P	D42	CSI 5 Data 0	Input	MIPI DPHY/CPHY
61	CSI5_D0_N	D43			
63	–	–	Ground	Ground	–
65	CSI5_CLK_P	C44	CSI 5 Clock	Input	MIPI DPHY/CPHY
67	CSI5_CLK_N	C45			
69	–	–	Ground	Ground	–
71	CSI5_D1_P	D46	CSI 5 Data 1	Input	MIPI DPHY/CPHY
73	CSI5_D1_N	D45			
75	I2C3_CLK	F53	Camera I2C	Bidir/OD	1.8V (3.3V tolerant)
77	I2C3_DAT	E53			
79	–	–	Ground	Ground	–
81 83	–	–	2.8V Analog Camera supply (see note)	Power	–
85	GPIO10	A62	Camera FRSYNC #1	Output	1.8V
87	I2C2_CLK	J61	General Purpose I2C #2	Bidir/OD	1.8V (3.3V tolerant)
89	I2C2_DAT	K61			
91	MCLK02	J54	Camera #0 Master Clock	Output	1.8V
93	UART4_CTS	L49	Camera #0 Powerdown	Output	1.8V
95	UART4_TX	L5	Camera #0 Reset	Output	1.8V
97	GPIO6	E59	Camera FRSYNC #3	Output	1.8V
99	–	–	Ground	Ground	–
101	–	–	Unused	Unused	–
103	SPI2_MOSI	F60	Camera Interrupt #3	Input	1.8V
105	I2C5_CLK	A53	General I2C #5	Bidir/OD	1.8V (3.3V tolerant)
107	I2C5_DAT	C53			
109 111 113	–	–	Unused	Unused	–
115	–	–	Ground	Ground	–
117	SPI2_CLK	E61	Camera Interrupt #1	Input	1.8V
119	GPIO12	E10	System power enable	Output	1.8V
2	CSI_1_D0_P	G41	CSI 1 Data 0	Input	MIPI DPHY/CPHY
4	CSI_1_D0_N	G42			
6	–	–	Ground	Ground	–
8	CSI_1_CLK_P	H43	CSI 1 Clock	Input	MIPI DPHY/CPHY
10	CSI_1_CLK_N	H42			
12	–	–	Ground	Ground	–
14	CSI_1_D1_P	J41	CSI 1 Data 1	Input	MIPI DPHY/CPHY
16	CSI_1_D1_N	J42			
18	–	–	Ground	Ground	–
20	CSI_3_D0_P	E45	CSI 3 Data 0	Input	MIPI DPHY/CPHY
22	CSI_3_D0_N	E44			

Pin #	Assoc. Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level
24	–	–	Ground	Ground	–
26	CSI_3_CLK_P	F46	CSI 3 Clock	Input	MIPI DPHY/CPHY
28	CSI_3_CLK_N	F45			
30	–	–	Ground	Ground	–
32	CSI_3_D1_P	G44	CSI 3 Data 1	Input	MIPI DPHY/CPHY
34	CSI_3_D1_N	G45			
36	–	–	Ground	Ground	–
38	CSI6_D0_P	K44	CSI 6 Data 0	Input	MIPI DPHY/CPHY
40	CSI6_D0_N	K43			
42	–	–	Ground	Ground	–
44	CSI6_CLK_P	J44	CSI 6 Clock	Input	MIPI DPHY/CPHY
46	CSI6_CLK_N	J45			
48	–	–	Ground	Ground	–
50	CSI6_D1_P	H46	CSI 6 Data 1	Input	MIPI DPHY/CPHY
52	CSI6_D1_N	H45			
54	–	–	Ground	Ground	–
56	–	–	DVDD_CAM_LV. Reserved for Low Voltage Digital Supply	(Power)	–
58					
60	CSI7_D0_P	A44	CSI 7 Data 0	Input	MIPI DPHY/CPHY
62	CSI7_D0_N	A45			
64	–	–	Ground	Ground	–
66	CSI7_CLK_P	B45	CSI 7 Clock	Input	MIPI DPHY/CPHY
68	CSI7_CLK_N	B46			
70	–	–	Ground	Ground	–
72	CSI7_D1_P	C47	CSI 7 Data 1	Input	MIPI DPHY/CPHY
74	CSI7_D1_N	C48			
76	GPIO14	L15	Camera Error #1	Input	1.8V
78	GPIO28	L9	Camera Error #2	Input	1.8V
80	–	–	Ground	Ground	–
82	–	–	2.8V Analog Camera supply (see note)	Power	–
84	GPIO29	A7	Camera Error #3	Input	1.8V
86	UART4_RTS	L4	Camera Error #4	Input	1.8V
88	MCLK03	H53	Camera #1 Master Clock	Output	1.8V
90	GPIO15	F10	Camera #1 Powerdown	Output	1.8V
92	GPIO16	F9	Camera #1 Reset	Output	1.8V
94	MCLK04	H55	Camera #2 Master Clock	Output	1.8V
96	GPIO13	G7	Camera FRSYNC #4	Output	1.8V
98	GPIO7	F59	Camera FRSYNC #2	Output	1.8V
100	–	–	Ground	Ground	–
102	–	–	1.8V Camera supply.	Power	–
104	SPI2_CS0_N	D60	Camera Interrupt #4	Input	1.8V
106	SPI2_MISO	D62	Camera Interrupt #2	Input	1.8V
108	–	–	3.3V supply	Power	–
110					

Pin #	Assoc. Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level
112 114	–	–	Unused	Unused	–
116	–	–	Ground	Ground	–
118 120	–	–	3.3V supply	Power	–

Notes:
1. The 2.8V supply supports up to 600mA total from all three pins.
2. In the Type/Dir column, Output is to camera module. Input is from camera module. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved/Unused

See the *Jetson AGX Orin Product Design Guide* for routing guidelines. The max trace lengths in the tables below take into account the routing length used on the carrier board.

Table 3-2. Camera Module CSI PCB Trace Allowances – DPHY

Speed	Max Trace Lengths Allowed on Camera Module (mm)
1.0 Gbps	345
1.5 Gbps	235
2.5 Gbps	80

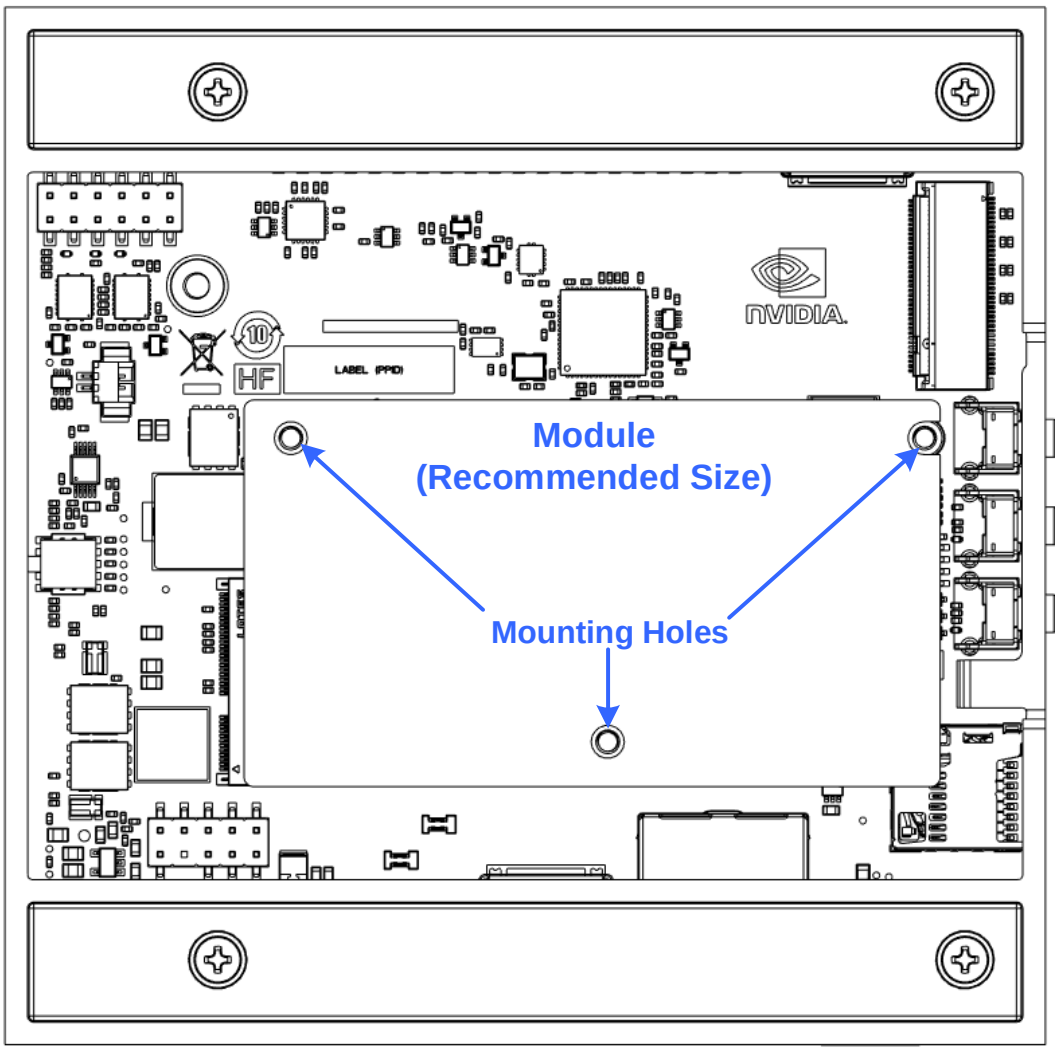
Note: Max trace delays and lengths assume CSI device is directly on the board that connects to the camera connector on the developer kit. If there is an additional connector between the camera connector and the end device, see the *Jetson AGX Orin OEM Product Design Guide* for additional limitations on speed and delay or length.

Table 3-3. Camera Module CSI PCB Trace Allowances – CPHY

Speed	Max Trace Lengths Allowed on Camera Module (mm)
1.5 Gsps	250
2.5 Gsps	130
3.5 Gsps	100

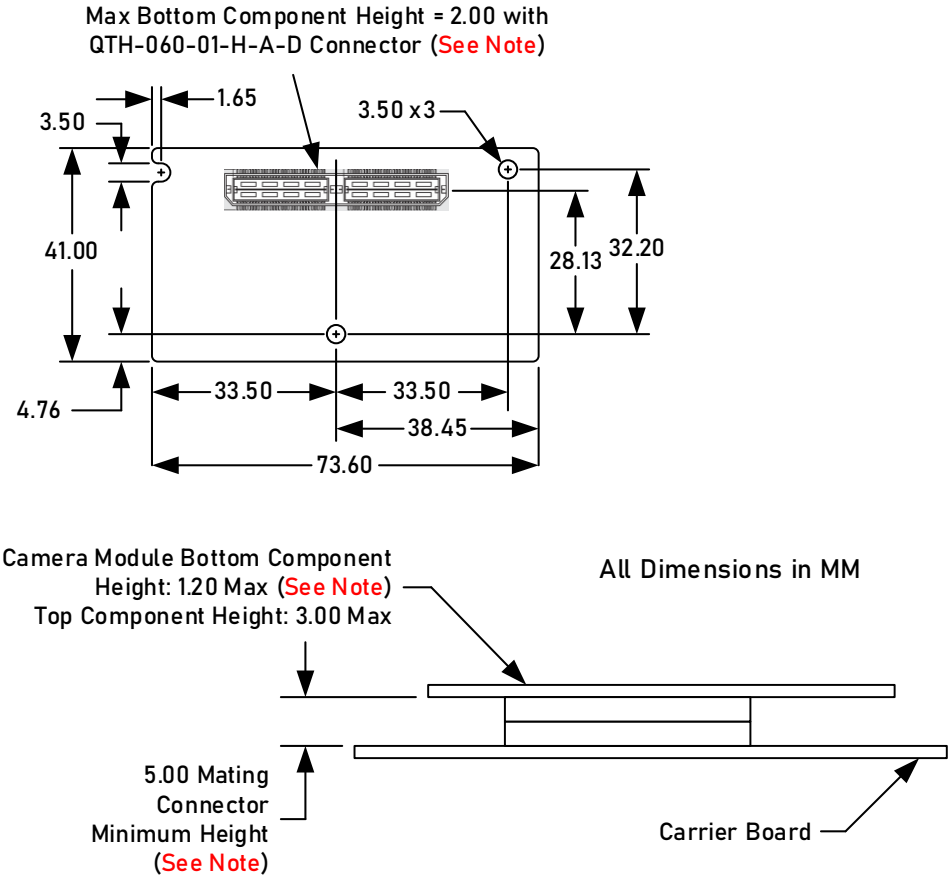
Note: See note under Table 3-2

Figure 3-1. Developer Kit with Recommended Module Size



Note: If a taller connector (≥ 25 mm) is used on the module, the developer kit casing will not conflict with the module regardless of size. See Figure 3-3 for details.

Figure 3-2. Module Dimensions Recommended Size

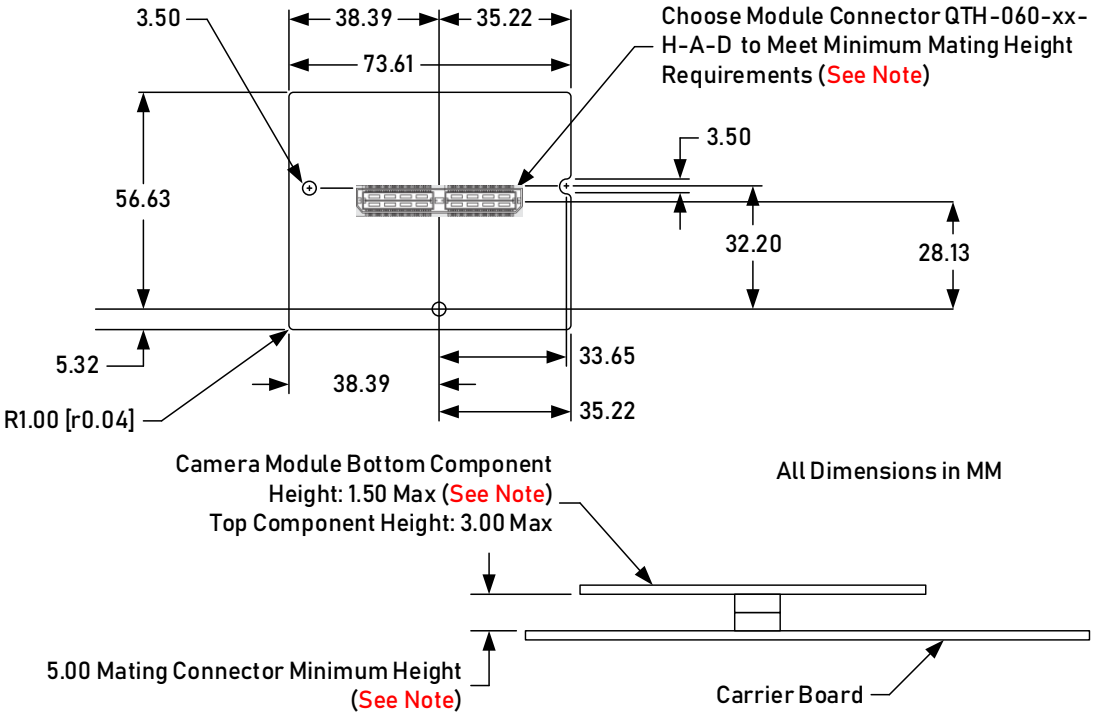


Note: The bottom component height maximum allowed depends on the camera module connector used.

- QTH-060-01-H-A-D (5.00 mm Spacing) = 1.2 mm maximum bottom component height
- QTH-060-02-H-A-D (8.00 mm Spacing) = 4.2 mm maximum bottom component height
- QTH-060-03-H-A-D (11.00 mm Spacing) = 7.2 mm maximum bottom component height
- QTH-060-04-H-A-D (16.00 mm Spacing) = 12.2 mm maximum bottom component height

A larger interposer board could be used with the Jetson AGX Orin Developer Kit carrier board but may not be compatible with future developer kits supporting the same connector. The mechanical limits shown in TBD will ensure the interposer module will fit on a Jetson AGX Orin and Jetson AGX Xavier Developer Kit carrier board if the mating connector used is the minimum height (QTH-060-01-H-A-D with 5.00 mm board to board spacing).

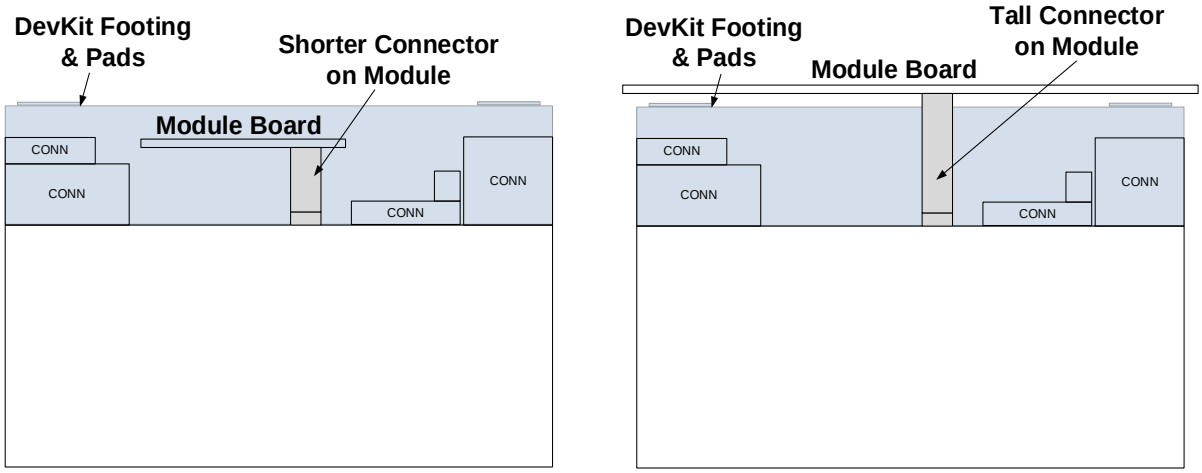
Figure 3-3. Mechanical Limits Interposer Module Outline



3.2.1 Module Connector Height Considerations

If a shorter connector, such as the Samtec QTH-060-04-H-D-A (which has a mating height of 16mm), is used, the module size is limited due to connectors and the developer kit footing and pads (see left example in the following figure). If a taller connector (mating height ≥ 25 mm), such as the Samtec QTH-060-07-F-D-A is used, then the module board will be above the obstructions and can be as large as needed (see right example in following figure).

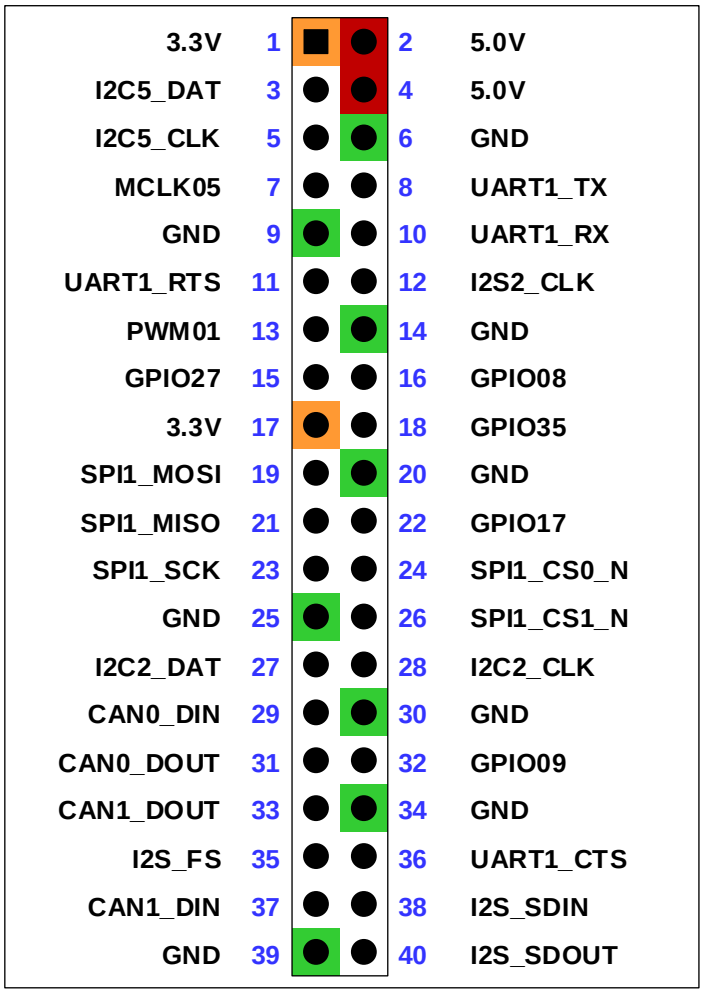
Figure 3-4. Module Connector Height Considerations



3.3 40-Pin Expansion Header

The Jetson AGX Orin carrier board includes a 40-pin (2 × 20, 2.54 mm pitch) expansion header (J30). The connector used on the carrier board is a Wieson G2100CE04C-009-H part.

Figure 3-5. 40-pin Expansion Header Top View



The 40-pin expansion connector includes various audio and control interfaces including:

- Audio: I2S, Digital Mic, Clock and Control
- I2C (2x), SPI, UART, CAN, and PWM (2x)
- GPIOs (dedicated as well as shared with other interface pins)

All the signal pins are 3.3V level.

Note: Many of the signals at the 40-pin Expansion Header come from TI TXB0108 level translators. Due to the design of these devices, the output drivers are very weak so they can be overdriven by another connected device output for bidirectional support. The signals associated with these buffers have a "3" in the note column of Table 3.4. See the Jetson Nano Developer Kit 40-pin Expansion Header GPIO Usage Considerations Application Note for more information.

Table 3-4. 40-Pin Expansion Header Pin Description

Pin #	Associated Module Pin Name	Module Pin #	SoC Pin Name	Usage & Description Primary / Secondary	Type/Dir	Max Current	SoC GPIO Port #	POR	PU/PD (KΩ) on Module	Notes
1	–	–	–	Main 3.3V Supply	Power	1A	–	–	–	1
2	–	–	–	Main 5.0V Supply	Power	1A	–	–	–	1
3	I2C4_DAT	E60	GP16_I2C8_DAT	General I2C #5 Data	Bidir/OD	±1mA	PDD.02	z	2.2 PU	2
4				Main 5.0V Supply	Power	1A	–	–	–	1
5	I2C4_CLK	D61	GP81_I2C9_CLK	I2C #5 Clock	Bidir/OD	±1mA	PDD.01	z	2.2 PU	2
6	–	–	–	Ground	Ground	–	–	–	–	–
7	MCLK05	L57	GP66	GPIO/ Clock	Bidir	±20uA	PQ.06	pd	–	3
8	UART1_TX	K53	GP70_UART1_TXD_ BOOT2_STRAP	GPIO/ UART	Output	±24mA	PR.02	pd	–	4
9	–	–	–	Ground	Ground	–	–	–	–	–
10	UART1_RX	K54	GP71_UART1_RXD	GPIO/ UART	Input	–	PR.03	pd	–	4
11	UART1_RTS	L51	GP72_UART1_RTS_N	GPIO/ UART	Output	±24mA	PR.04	pd	–	4
12	I2S2_CLK	G4	GP122	GPIO/ I2S	Bidir	±20uA	PH.07	pd	–	3
13	PWM01	K57	GP68	GPIO	Bidir	±20uA	PR.00	pd	–	3
14	–	–	–	Ground	Ground	–	–	–	–	–
15	GPIO27	H52	GP88_PWM1	GPIO/ PWM	Bidir	±20uA	PN.01	z	–	3
16	GPIO08	B62	GP25	GPIO/ Digital Mic Data	Input	±1mA	PBB.01	pd	–	5
17	–	–	–	Main 3.3V Supply	Power	1A	–	–	–	1
18	GPIO35	L50	GP115	GPIO/ PWM	Output	±20uA	PH.00	z	–	3, 7
19	SPI1_MOSI	D55	GP49_SPI1_MOSI	GPIO/ SPI	Bidir	±20uA	PZ.05	pd	–	3
20	–	–		Ground	Ground	–	–	–	–	–
21	SPI1_MISO	A56	GP48_SPI1_MISO	GPIO/ SPI	Bidir	±20uA	PZ.04	pd	–	3
22	GPIO17	A54	GP56	GPIO	Bidir	±20uA	PP.04	pd	–	3
23	SPI1_CLK	J57	GP47_SPI1_CLK	GPIO/ SPI	Bidir	±20uA	PZ.03	pd	–	3
24	SPI1_CS0_N	E55	GP50_SPI1_CS0_N	GPIO/ SPI	Bidir	±20uA	PZ.06	z	–	3
25	–	–	–	Ground	Ground	–	–	–	–	–
26	SPI1_CS1_N	B56	GP51_SPI1_CS1_N	GPIO/ SPI	Bidir	±20uA	PZ.07	z	–	3
27	I2C2_DAT	K61	GP14_I2C2_DAT	I2C #2 Data/ GPIO	Bidir/OD	±1mA	PDD.00	z	2.2 PU	2
28	I2C2_CLK	J61	GP13_I2C2_CLK	I2C #2 Clock/ GPIO	Bidir/OD	±1mA	PCC.07	z	2.2 PU	2
29	CAN0_DIN	F58	GP18_CAN0_DIN	GPIO/ CAN	Input	±1mA	PAA.01	z	–	5
30	–	–	–	Ground	Ground	–	–	–	–	–
31	CAN0_DOUT	D59	GP17_CAN0_DOUT	GPIO/ CAN	Output	±1mA	PAA.00	z	–	5

Pin #	Associated Module Pin Name	Module Pin #	SoC Pin Name	Usage & Description Primary / Secondary	Type/Dir	Max Current	SoC GPIO Port #	POR	PU/PD (KΩ) on Module	Notes
32	GPIO09	C61	GP26	GPIO/ Digital Mic Clock	Bidir	±1mA	PBB.00	pd	–	5
33	CAN1_DOUT	H61	GP19_CAN1_DOUT	GPIO/ CAN	Output	±1mA	PAA.02	z	–	5
34	–	–	–	Ground	Ground	–	–	–	–	–
35	I2S2_FS	E4	GP125	GPIO/ I2S	Bidir	±20uA	PI.02	pd	–	3
36	UART1_CTS	H54	GP73_UART1_CTS_N	GPIO/ UART	Input	–	PR.05	pd	–	4
37	CAN1_DIN	B61	GP20_CAN1_DIN	GPIO/ CAN	Input	±1mA	PAA.03	z	–	5
38	I2S2_DIN	F6	GP124	GPIO/ I2S	Input	±20uA	PI.01	pd	–	3, 7
39	–	–	–	Ground	Ground	–	–	–	–	–
40	I2S2_DOUT	F5	GP123	GPIO/ I2S	Output	±20uA	PI.00	pd	–	3, 7

Notes:
1. This is current capability per power pin.
2. These pins connect to the SoC through a FXMA2102L8X level shifter. They are open-drain (either pulled up, or driven low by the SoC when configured as outputs). The max drive that meets the data sheet VOL is 1mA.
3. See related note above table.
4. These pins connect to a SN74LVC4T245 buffer.
5. These pins are directly connected to the SoC. The max drive that meets full data sheet VOL/VOH is 1mA.
6. For power-on default, "pd" = SoC Internal Pull-down, "pu" - SoC Internal pull-up, and "z" – Tristate
7. In the Type/Dir column, Output is to expansion header. Input is from expansion header. Bidir is for bidirectional signals.
8. The direction indicated matches that indicated in the reference design schematics. These signals support GPIO functionality and can be bidirectional.

Legend	Ground	Power

3.4 Fan Control

The Jetson carrier board includes a 4-pin, 1.25 mm pitch fan header (J9). The connector on the carrier board is an Aces Electronics 50279-0040N-003 device.

Table 3-5. Fan Connector Pin Description

Pin #	Connector (Codec) Pin Name	Associated Module Pin Name[1]	Module Pin #	Usage/Description	Type/Dir	Voltage Level
1	GND	–	–	Ground	Ground	–
2	PWR	–	–	5.0V Supply (VDD_5V)	Power	5V
3	TACH	FAN_TACH	E54	Fan Tachometer signal	Input	1.8V
4	PWM	FAN_PWM	K62	Fan Pulse Width Modulation signal	Output	5V

Note: In the Type/Dir column, Output is to Audio Header. Input is from Audio Header. Bidir is for bidirectional signals.

Legend	Ground	Power

3.5 Automation Header

The Jetson carrier board includes a 12-pin, 2.54 mm pitch header (J42) that makes accessible several critical system control signals. The connector used on the carrier board is a Wieson AC2100-0011-019-HH part.

Table 3-6. Automation Header Description

Pin #	Associated Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level
1	–	–	Ground	Ground	–
2	FORCE_RECOVERY_N	L10	Force Recovery Strap	Input	1.8V
3	SYS_RESET_N	L60	System Reset – Connected to Reset Button on carrier board	Input	1.8V
4	–	–	Power Button On – Connected to Power Button on carrier board	Input	3.3V
5	–	–	Output from USB Type C PD Controller (See note 1)	Output	3.3V
6	–	–	ACOK (USB Type C or DC Jack power OK). To button power-on controller.	Input	3.3V
7	MODULE_SLEEP_N	J60	Carrier board sleep	Output	1.8V
8	SYSTEM_OC_N	A61	System Overcurrent indicator	Input	1.8V
9	GPIO38	A47	Wake on LAN (WOL)	Input	3.3V
10	–	–	Ground	Ground	–
11	JTAG_TRST_N		JTAG Test Reset	Input	1.8V
12	–	–	Ground	Ground	–

Notes:

1. Auto-Power-On is enabled when Pin 5 and Pin 6 are tied together.
2. In the Type/Dir column, Output is to header. Input is from header. Bidir is for bidirectional signals.

Legend | Ground | Power |

3.6 DC Power Jack

The Jetson carrier board includes a DC power jack (J41) as an alternative to using the included USB Type C power supply. The jack used on the carrier board is a Wieson Technologies AC0002-0011-001-HH part. This has a center pin that is 2.5 mm in diameter and accepts a barrel plug with an outside diameter of 5.5 mm.

Table 3-7. DC Jack Pin Description

Pin #	Usage/Description	Type/Dir
1	Option for Main DC input supplying SYS_VIN_HV	Power
2	Ground	Ground
3	Ground	Ground
4	Ground	Ground

Legend	Ground	Power

3.7 RTC Backup Battery Connector

The Jetson carrier board has a connector where a Real Time Clock (RTC) backup battery can be connected. This connector (J13) is commonly used on laptop designs. The connector used is a Wieson Technologies AC2651-0011-003-HH, 2-pin, 1.25 mm pitch connector.

Table 3-8. RTC Backup Battery Connector Pin Description

Pin #	Associated Module Pin Name	Module Pin #	Usage/Description	Type/Dir
1	PMIC_BBATT	D37	Real-Time-Clock backup battery supply	Power
2	–	–	Ground	Ground

Legend	Ground	Power

Chapter 4. Miscellaneous

4.1 Buttons, Jumpers, and Indicators

Table 4-1 and Table 4-2 describe the buttons (switches), jumpers, and LED indicators.

Table 4-1. Buttons

Button	Description	Usage
S1	Power button on	Used to power system up if OFF or put in sleep mode ON. If held for >10 seconds, the system will shut down.
S2	Reset button	Used to force a full system reset.
S3	Force Recovery button	Used to enter Force Recovery Mode. Button is held down while either system is first powered on, or by pressing and releasing reset button while recovery button is pressed.

Table 4-2. LED Indicators

LED	Description	Usage
DS2	SOC Regulator Power LED (Green)	Indicates when the main 5.0V (VDD_5V) supply is enabled

4.2 I2C Interface Usage

The following tables show the I2C usage on the Jetson AGX Orin module and developer kit carrier board.

Table 4-3. Jetson AGX Orin I2C Interface Usage

Ctrl	Module Pin Names (Orin Pins)	Usage on Module	I2C Address	On-Module Pull-up/voltage
I2C1	I2C1_CLK/DAT	ID EEPROM	7'h50	1KΩ to 1.8V
I2C2	I2C2_CLK/DAT	Current Monitors	7'h40 and 7'h41	1KΩ to 1.8V (also current monitors via 1.8V-5V level shifters w/10k pull-ups to 5V)
I2C3	I2C3_CLK/DAT			1KΩ to 1.8V
I2C4	DP1_AUX_CH_N/P			1KΩ to 1.8V
I2C6	DP2_AUX_CH_N/P			None
I2C7	DP0_AUX_CH_N/P			1KΩ to 1.8V
I2C8	I2C4_CLK/DAT			1KΩ to 1.8V
I2C9	I2C5_CLK/DAT			1KΩ to 1.8V

Table 4-4. Jetson AGX Orin Developer Kit Carrier Board I2C Interface Usage

Ctrlr	Module Pin Names (Orin Pins)	Usage on Carrier Board	I2C Address	On-Module Pull-up/voltage
I2C1	I2C1_CLK/DAT	ID EEPROM	7h56	1KΩ to 1.8V
I2C2	I2C2_CLK/DAT	Camera Connector 12V DC-DC USB PD Controller USB Hub M.2 Key M. 40-pin Connector	 7'h74 7'h08 7h6A	1KΩ to 1.8V (also Current Monitors via 1.8V-5V level shifters w/10k pull-ups to 5V)
I2C3	I2C3_CLK/DAT	PCIe Connector Camera Connector		1KΩ to 1.8V
I2C4	DP1_AUX_CH_N/P		7'h1A	1KΩ to 1.8V
I2C6	DP2_AUX_CH_N/P	DP Connector		None
I2C7	DP0_AUX_CH_N/P			None
I2C8	I2C4_CLK/DAT	40-pin Connector		1KΩ to 1.8V
I2C9	I2C5_CLK/DAT	Camera Connector, Audio Codec M.2 Key E connector (not connected by default)	0x34	1KΩ to 1.8V

Chapter 5. Mechanicals

Figure 5-1 and Figure 5-2 show the mechanical dimensions for the carrier board.

Figure 5-1. Developer Kit Carrier Board Dimensions – Top View

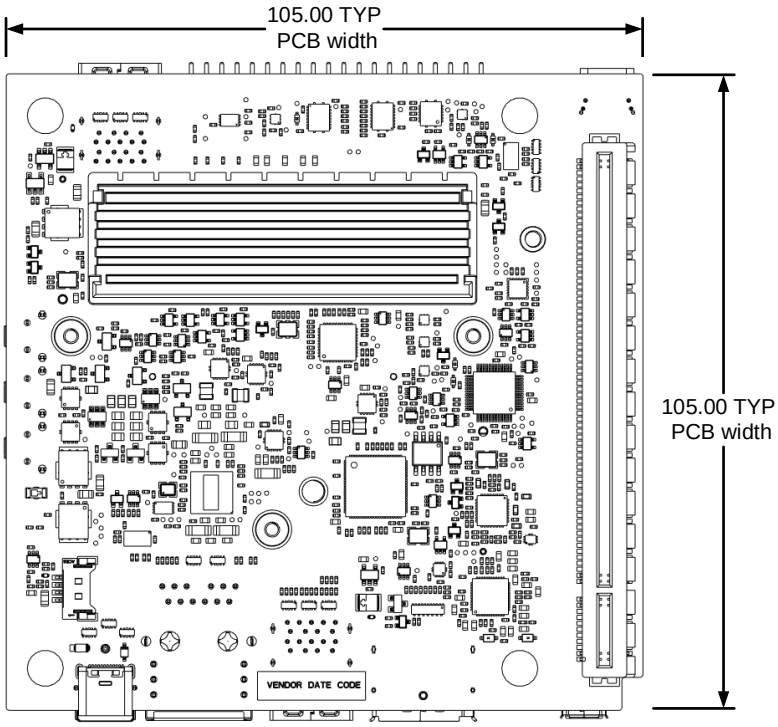


Figure 5-2. Developer Kit Carrier Board Mechanical Dimensions – Side View

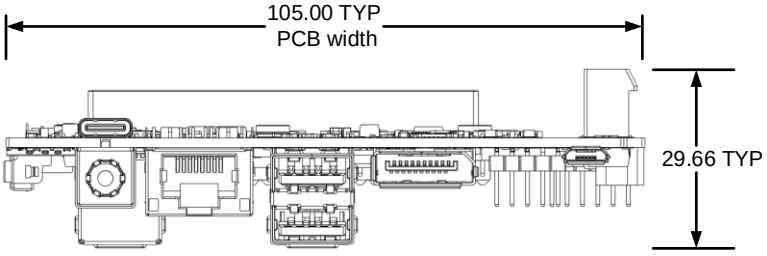
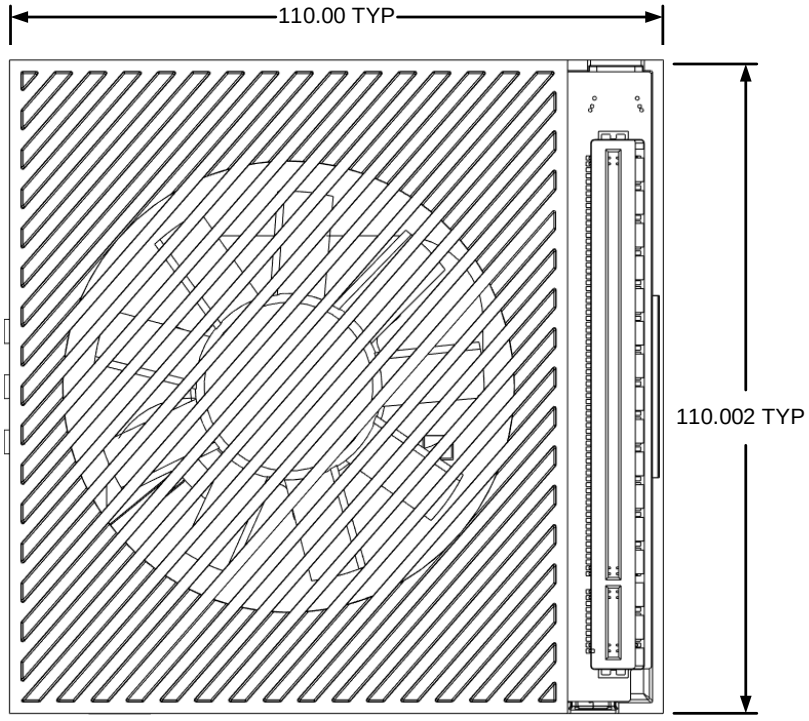


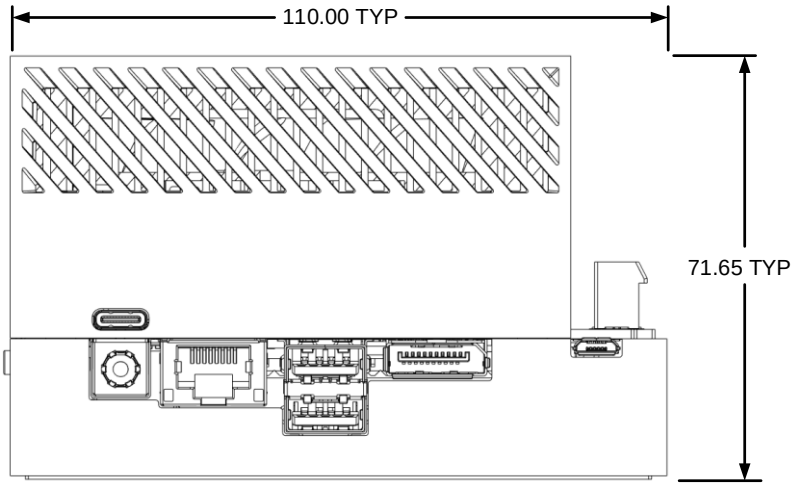
Figure 5-3 and Figure 5-4 show the mechanical dimensions for the carrier board. The weight of the DevKit is 872.5 grams.

Figure 5-3. Developer Kit Mechanical Dimensions – Top View



Note: The PCIe cover is not shown in Figure 5-2.

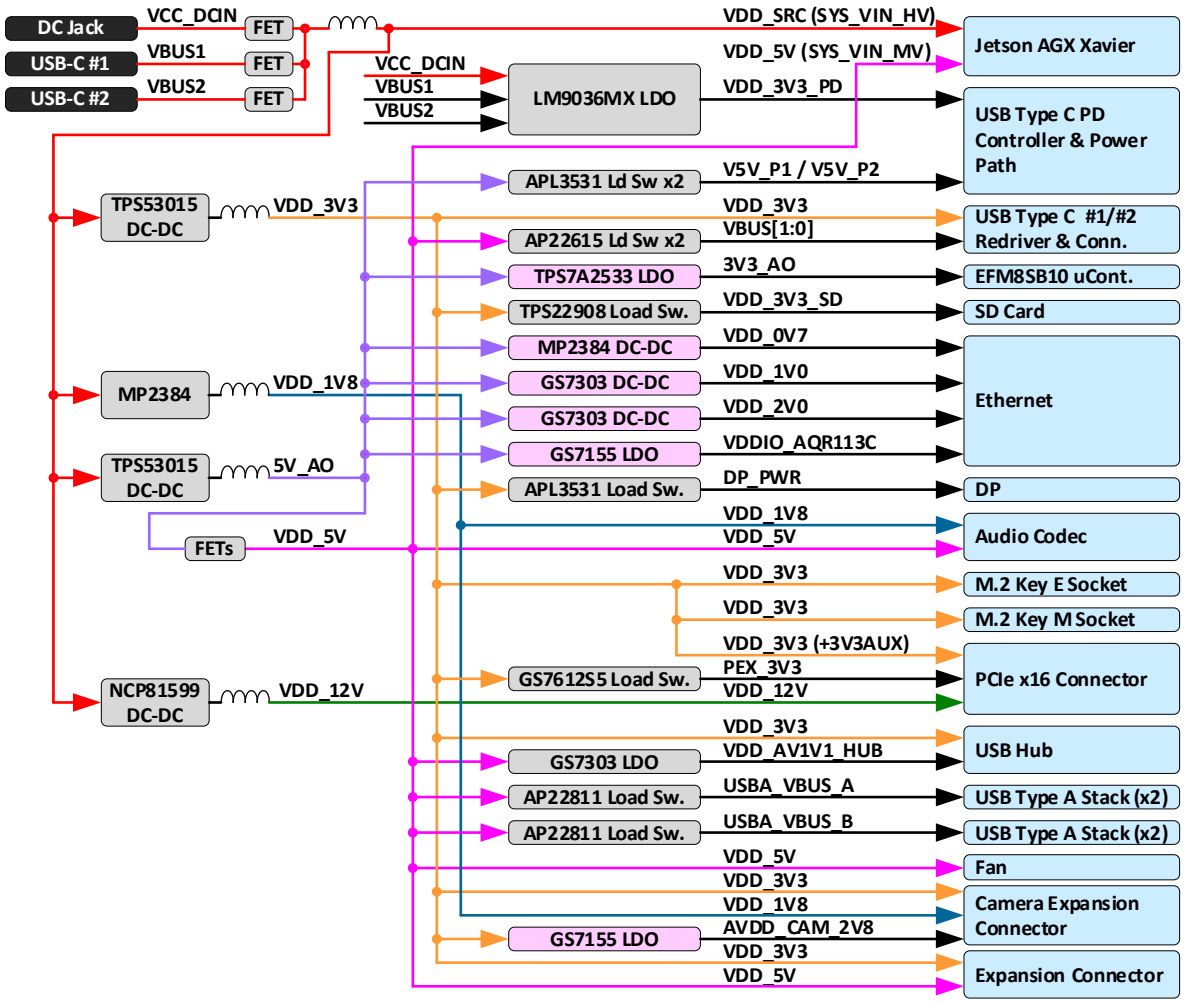
Figure 5-4. Developer Kit Mechanical Kit – Side View



Chapter 6. Interface Power

Figure 6-1 shows the interface connector power diagram.

Figure 6-1. Interface Connector Power Diagram



The following tables show the allocation of supplies to the connectors on the Jetson carrier board and current capabilities.

Table 6-1. Interface Power Supply Allocation

Power Rails	Usage	(V)	Power Supply or Gate	Source	Enable
VCC_SRC	Main power input from DC Adapter or USB type C VBUS[2:1]	7-20	FETs	DC Adapter or Type C USB	
VDD_3V3_PD		3.3	LM9036MX LDO	VCC_DCIN/VBUS[2:1]	VCC_DCIN, VBUS[2:1]
5V_AO	Always-on 5V supply	5.0	TPS53015 DC-DC	VCC_SRC	VDD_5V
VDD_5V	Main 5V supply	5.0	FETs	5V_AO	VIN_PWR_ON
VDD_3V3	Main 3.3V supply	3.3	TPS53015 DC-DC	VCC_SRC	CARRIER_PWR_ON
3V3_AO	Always On 3.3V supply	3.3	TPS7A2533	5V_AO	5V_AO PG
VDD_1V8	Main 1.8V supply	1.8	MP2384 DC-DC	VCC_SRC	CARRIER_PWR_ON
VDD_12V	12V rail for PCIe, Fan	12.0	NCP81599 DC-DC	VCC_SRC	Module GPIO28
USB[2:1]_VBUS	VBUS pin from USB Type C connectors (alternative is DC Jack)	5-20	AP22615 Ld Sw (x2)	VCC_USBPD	PD Controller
PEX_3V3	PCIe x16 connector +3V3 rail supply	3.3	GS7612S5 Load Switch	VDD_3V3	Module GPIO29
VDD_AV1V1_HUB	USB Hub controller rail	1.1	GS7303	VDD_5V	VDD_3V3 PG
USBA_VBUS_A	USB Type A stack VBUS (J24)	5.0	AP22811 Load Switch	VDD_5V	Hub Power Enable
USBA_VBUS_B	USB Type A VBUS (J27/J29)	5.0	AP22811 Load Switch	VDD_5V	Hub Power Enable
VDD_3V3_SD	SD Card power rail	3.3	APL3531S6I Power Switch	VDD_3V3	Module UART5_RTS
VDD_0V7	Ethernet PHY 0.7V power rail	0.7	MP2384 DC-DC	5V_AO	VDD_1V8 PG
VDD_1V0	Ethernet PHY 1.0V power rail	1.0	GS7303 DC-DC	5V_AO	VDD_0V7 supply PG
VDD_2V0	Ethernet PHY 2.0V power rail	2.0	GS7303DC-DC	5V_AO	VDD_1V0 supply PG
VDDIO_AQR113C	Ethernet PHY I/O rail (1.8V)	1.8	GS7155 LDO	5V_AO	VDD_2V0 supply PG
DP_PWR	3.3V rail for DP connector	3.3	APL3531S6I Power Switch	VDD_3V3	Module GPIO20
AVDD_CAM_2V8	Camera Analog power rail	2.8	GS7155	VDD_3V3	Module GPIO18

Table 6-2. Interface Supply Current Capabilities

Power Rails	Usage	(V)	Max Current (A)
VCC_SRC	Main power input from USB Type C connectors or DC Jack	7-20	5.0
VDD_5V	Main system 5V supply	5.0	11
VDD_3V3	Main system 3.3V supply	3.3	10
VDD_1V8	Main system 1.8V supply	1.8	3.5
VDD_12V	12V rail for PCIe connector & optionally for Fan	12	5.5
AVDD_CAM_2V8	Analog Camera rail	2.8	3.0

Notes:

1. The values shown in the "Max Current" column indicate the total power available on the expansion connectors minus the current used on the platform (not per connector pin).
2. If a given voltage rail cannot provide enough current, a possible solution is for the user to use a regulator from one of the rails that has extra capacity to generate the desired rail.

Table 6-3. Supply Current Capabilities per Connector per Supply

Power Rails	Connector	(V)	Max Allocated Current (A)
VDD_12V	Fan (optional)	12	0.45
	PCIe		3.0
VDD_5V	40-pin	5	1.0
	Fan (default)		0.15
VDD_3V3	PCIe 3.3V Aux	3.3	1.0
	Camera		1.44
	M.2 Key M		0.93
	M.2 Key E		0.8
PEX_3V3	PCIe 3.3V	3.3	3.0
AVDD_CAM_2V8	Camera	2.8	0.6
VDD_1V8	Camera	1.8	1.72

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