Jetson AGX Orin Series

Design Guide

DG-10653-001_v1.6 | June 2023

Document History

DG-10653-001_v1.6

Version	Date	Description of Change
1.0	March 15, 2022	Initial release
1.1	June 24, 2022	Power • Power On Sequence (Power Button Case) Figure: Updated to include sequence between SYS)VIN_MV/HV and added additional timing. • Power Down Sequence (Controlled Case) Figure: Updated to include sequence between SYS)VIN_MV/HV and added additional timing. • SYS_VIN_HV Input Section: Update to include note related to PD controller used in reference design. USB, PCIe, MGBE • USB, PCIe and MGBE Section: Updated to remove support for UFS and reduced MGBE support to a single MGBE IF. • USB 3.2, PCIe, and MGBE Mapping Options Table: Updated to remove Configuration #3 and corrected PCIe IF width for UPHY0[7:4]. • Simple USB Type A Connection Example Figure: Corrected SoC pin names for USB 2.0 pins. • USB Type C Connection Example Figure: Corrected SoC pin names for USB 2.0 pins. Display • DP and eDP Main Link Signal Routing Requirements Table: Updated Resonance dip frequency to include separate HBR2 and HBR3 requirements. Video Input • CSI Configurations for C-PHY Figures: Updated title for x2 and x4 figure and added Table 9-5 for x1 and x3 configurations. • Camera CSI C-PHY Connections Figure: Updated to include x3 and x1 combinations.
1.2	October 18, 2022	• Table 1-2: Added note under table clarifying USB 3.2 naming. • Figure 5-1: Added MODULE_SHDN_N • Table 5-1: > Update PMIC_BBAT voltage range to be 1.85V-5.5V and added note in Usage/Description clarifying this is input only. > Updated usage/description and direction for MODULE_SHDN_N > Updated usage/description for POWER_BTN_N • Figure 5-1: > Added MODULE_SHDN_N

Version	Date	Description of Change
		> Added PRSNT[1:0] pins including note • Section 5.1: Updated description of powerdown sequence to match updated figure. • Section 5.3.1: Updated note to include MODULE_SHDN_N. • Table 5-2: Updated Description for ACOK. • Figure 5-6: Updated pull-up value on MODULE_SHDN_N and added PRSNT[1:0] and associated note. • Section 5.3.2.1: Update button power MCU "Defined behavors" section. • Section 5.3.2.2: Updated text describing what happens to FORCE_SHUTDOWN_N and CARRIER_POWER_ON when Power-on is successful. • Section 5.3.2.4: Updated to include comment related to ACOK. • Section 7.1: Updated intro paragraph to USB section. • Figure 7-2: Updated figure to show the signal going to I2C_INT_CCG4 passing through level shifter and changed module pin used for this. • Figure 7-4: Corrected module pin on End Point side for refclk coming from Rootport side. • Figure 7-4: Updated to show pull-up required on INT_0. • Table 11-3: Updated SD/SDIO max lengths/skews • Figure 14-1: Remove SPI5 which is not supported.
1.3	April 6, 2023	• Section 1.2: Added Layout Checklist to Attachments list. • Table 2-3: Updated J62 as RSVD but should be connected to GND by 0ohm resistor on carrier board. • Section 3.4: Updated mounting screw torque in Step 4. • Updated Section 5.1: Power Sequencing completely. • Updated UHPY Tables: Table 7-4, Table 7-5, Table 7-6: > Split UPHY mapping options into separate tables per UPHY block > Updated text above tables allowing more configuration flexibility. > Separated RP and EP into separate configurations within tables. • Section 7.1: Added support for polarity inversion for USB 3.2 ports. • Figure 7-4, Table 7-15: Added PCIe Endpoint connection figure and table. • Figure 7-5: Corrected TX/RX swap of module pins for Root Port. • Table 7-16: > Updated with details of supported PCIe interfaces instead of generic connections. > Added RX/TX and REFCLK connections rows. > Removed mention of support for C6 in note under table.

Version	Date	Description of Change
		• Table 7-18: Updated table to include more connection details. • Figure 9-1: Added level shifter detail breakout. • Figure 9-2/Table 9-3: Added DP connection example with PI3AUX221 device. • Figure 9-4: Added DP_AUX and CEC gating example breakouts. • Table 9-6: Updated Termination column. • Table 10-7: Removed mention of PSFEXT and related note. • Table 10-7: Updated CSI CPHY PCB type used as loss example and max lengths. • Table 16-3: Updated max data rate and corrected CAN SKU (called max length in error)
1.4	April 28, 2023	• Updated Excel spreadsheet attachment: Jetson_AGX_Orin_Series_Pin_Descriptions. • Updated the following parts of the document to change L53 from RSVD to RSVD (VIN_SYS_SV) and require connecting to 3.3V supply to be compatible with future Industrial modules: > Table 2-3: Connector Pinout Matrix Part 2: Columns G-L. > Introduction in Chapter 5: Power. > Table 5-1: Power and System Pin Descriptions. > Figure 5-1: Power Block Diagram. > Section 5.1: Power Sequencing. • Updated Figure 5-8 and Figure 5-9 for changes related to SYS_VIN_SV. • Updated Table 5-3: Power-OFF to On Timing Power Button Case and Table 5-4: Power-OFF to On Timing Auto Power-On Case with T_SV timing information.
1.5	May 10, 2023	• Updated Excel spreadsheet attachment: Jetson_AGX_Orin_Series_Pin_Descriptions. • Updated Chapter 1: Added note in the introduction to include JAOi. • Updated the following sections to change L53 from RSVD (VIN_SYS_SV) to VIN_SYS_SV for JAOi: > Table 2-3: Table 2-3.Connector Pinout Matrix Part 2: Columns G-L. > Introduction in Chapter 5: Power. > Table 5-1: Power and System Pin Descriptions. > Figure 5-1: Power Block Diagram. • Updated Section 5.1: Power Sequencing.

Version	Date	Description of Change
1.6	June 26, 2023	• Updated attachment: Jetson_AGX_Orin_Series_Schematic_Checklist.nvxlsx • Added a CAUTION text box regarding the 699-pin connector on the carrier board to Section 3.1: Connector Pin Orientations. • Updated Section 5.1: Power Sequencing including figures; changed signal name in power sequences from MOD_SHUTDOWN_N to MODULE_SHDN_N • Updated Figure 9-4: HDMI Connection Example; added connection from MODULE_SLEEP_N to 3.3V load switch to generate the enable for the HDMI 5V supply and the FET to 499 ohm termination resistors. • Updated UART max baud rate to be 4.25 Mbps in Table 15-3: UART Interface Signal Routing Requirements.

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Chapter 1. Introduction

This design guide contains recommendations and guidelines for engineers to follow and create a product that is optimized to achieve the best performance from the interfaces supported by the NVIDIA® Jetson™ AGX Orin series module, hereafter referred to as "Orin Module."

This design guide provides detailed information on the capabilities of the hardware module, which may differ from supported configurations by provided software. Refer to the software release documentation for information on supported capabilities.

> **!** IMPORTANT: References to Jetson AGX Orin (JAO) applies to any of the Jetson AGX Orin series of modules including Jetson AGX Orin Industrial (JAOi) except where explicitly noted.

> **!** IMPORTANT: Throughout the design guide, references to Master and Slave configurations have been updated to Initiator and Target respectively.

1.1 References

Refer to the following documents or models listed for more information. Always use the latest revision of all documents.

- *Jetson AGX Orin Series Data Sheet*
- *Orin Processors Technical Reference Manual*
- *Jetson AGX Orin Developer Kit Carrier Board Specification*
- *Jetson AGX Orin Series Pinmux Configuration Template*
- *Jetson AGX Orin Series Thermal Design Guide*
- *Jetson AGX Orin Developer Kit Carrier Board Design Files*
- *Jetson AGX Orin Developer Kit Carrier Board BOM*
- *Jetson AGX Orin Series Supported Component List*

1.2 Attachments

The following files are attached to this design guide.

- Jetson_AGX_Orin_Series_Pin_Descriptions.nvxlsx
- Jetson_AGX_Orin_Series_Schematic_Checklist.nvxlsx
- Jetson_AGX_Orin_Series_Layout_Checklist.nvxlsx
- Jetson_AGX_Orin_Bringup_Checklist.nvxlsx

To access the attached files, click the **Attachment** icon on the left-hand toolbar on this PDF (using Adobe Acrobat Reader or Adobe Acrobat). Select the file and use the Tool Bar options (**Open, Save**) to retrieve the documents.

Note that Excel files with the .nvxlsx extension will need to be saved as .xlsx.

1.3 Abbreviations and Definitions

Table 1-1 lists abbreviations that may be used throughout this design guide and their definitions.

Table 1-1. Abbreviations and Definitions

Abbreviation	Definition
CEC	Consumer Electronic Control
CAN	Controller Area Network
DP	VESA® DisplayPort® (output)
eDP	Embedded DisplayPort
eMMC	Embedded MMC
HDMI™	High Definition Multimedia Interface
I2C	Inter IC
I2S	Inter IC Sound Interface
LDO	Low Dropout (voltage regulator)
LPDDR5	Low Power Double Data Rate DRAM, Fifth-generation
MGBE	Multi-Gigabit Ethernet
PCIe (PEX)	Peripheral Component Interconnect Express interface
PDM	Pulse-Density Modulation
PHY	Physical Layer
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real Time Clock
SC7	System Core State 7 (Sleep)
SDIO	Secure Digital I/O Interface
SPI	Serial Peripheral Interface

Abbreviation	Definition
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

Table 1-2. Industry Standards

Interface	Specification
CAN	Version 2.0/ISO11898
DP	Version 1.4a
eDP	Version 1.4
ETHER_QOS	RGMII Version 2.0
HDMI	Version 2.1
I2C	NXP 3.0
MGBE	IEEE 802.3-2015
MIPI CSI	C-PHY Revision 2.0 / D-PHY 2.1
PCI Express	PCI Express Base Specification Revision 4.0, Version 1.0
SD/SDIO	SD: Version 4.2. SDIO: Version 4.1 (no UHS-II support)
USB	Universal Serial Bus Specification Revision 2.0, 3.2; Gen1 and Gen2
XFI	SFF INF-8077i, Revision 4.5, 2005

Note: All occurrences of USB 3.2 refer to "USB 3.2 Gen 1x1: SuperSpeed USB 5 Gbps" and "USB 3.2 Gen 2x1: SuperSpeed USB 10 Gbps" only. Also note that Gen 1x1 and Gen 2x1 are referred to simply as Gen1 and Gen2 in this design guide.

Chapter 2. NVIDIA Jetson AGX Orin

The NVIDIA Jetson AGX Orin series modules reside at the center of the embedded system solution and includes:

- Power (Power Sequencer, Regulators, and so on)
- DRAM (LPDDR5)
- QSPI NOR, Secure NOR, eMMC
- Power Monitors
- Thermal Sensor

Table 2-1. Orin Module Features

Category	Function		Category	Function
USB	USB 2.0 USB 3.2 Gen2x1 (10 Gbps)		Display	HDMI / DP (1x – see note). DP supports multi-head operation through MST.
PCIe	Root Port and Endpoint supported up to Gen4.		SPI	Initiator and Target
Camera	CSI (6x2 or 4x4) D-PHY and C-PHY		Fan	PWM and TACH
LAN	Gigabit Ethernet: RGMII I/F MGBE Ethernet: (USXGMII, XFI, SFI)		Debug	JTAG and UART
SD Card	SD card or SDIO		System	Power control, Reset, Alerts
Audio	I2S, Digital Mic and Speaker IFs		Power	Main Inputs (HV and MV)
Miscellaneous	CAN, I2C, UART			

Note: HDMI and DP share the same pins. See Chapter 9: Display for display details.

Table 2-2. Connector Pinout Matrix Part 1: Columns A-F

	A	B	C	D	E	F
01			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV
02			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV
03	PRSNT0/GND_LOOP_0	SYS_VIN_HV	GND	SYS_VIN_HV	GND	SYS_VIN_HV
04	SDCARD_D2	GND	RGMII_RD0	GND	I2S2_FS	GND
05	SDCARD_CMD	RGMII_TXC	RGMII_RXC	RGMII_RX_CTL	RGMII_RD3	I2S2_DOUT
06	UFS0_REF_CLK	SDCARD_CLK	UFS0_RST_N	SDCARD_D3	RGMII_SMA_MDC	I2S2_DIN
07	GPIO29	GND	I2S1_SDOUT	GND	RGMII_SMA_MDIO	GND
08	PEX_WAKE_N	GPIO11	PEX_C5_CLKREQ_N	I2S1_FS	SDCARD_D0	SDCARD_D1
09	GND	PEX_C1_RST_N	GND	PEX_C1_CLKREQ_N	GND	GPIO16
10	USB2_P	RSVD	USB1_N	PEX_C0_RST_N	GPIO12	GPIO15
11	USB2_N	GND	USB1_P	GND	PEX_C0_CLKREQ_N	GND
12	GND	UPHY_RX10_P	GND	UPHY_RX11_P	GND	USB0_P
13	GND	UPHY_RX10_N	GND	UPHY_RX11_N	GND	USB0_N
14	UPHY_RX8_N	GND	UPHY_RX9_N	GND	PEX_CLK0_N	GND
15	UPHY_RX8_P	GND	UPHY_RX9_P	GND	PEX_CLK0_P	GND
16	GND	UPHY_RX6_P	GND	UPHY_RX7_P	GND	PEX_CLK1_P
17	GND	UPHY_RX6_N	GND	UPHY_RX7_N	GND	PEX_CLK1_N
18	UPHY_RX4_P	GND	UPHY_RX5_N	GND	PEX_CLK2_N	GND
19	UPHY_RX4_N	GND	UPHY_RX5_P	GND	PEX_CLK2_P	GND
20	GND	UPHY_RX2_N	GND	UPHY_RX3_P	GND	PEX_CLK3_P
21	GND	UPHY_RX2_P	GND	UPHY_RX3_N	GND	PEX_CLK3_N
22	UPHY_RX0_P	GND	UPHY_RX1_N	GND	PEX_CLK4_N	GND
23	UPHY_RX0_N	GND	UPHY_RX1_P	GND	PEX_CLK4_P	GND
24	GND	UPHY_RX13_N	GND	UPHY_RX12_P	GND	PEX_CLK5_P
25	GND	UPHY_RX13_P	GND	UPHY_RX12_N	GND	PEX_CLK5_N
26	UPHY_RX15_P	GND	UPHY_RX14_N	GND	UPHY_REFCLK1_N	GND
27	UPHY_RX15_N	GND	UPHY_RX14_P	GND	UPHY_REFCLK1_P	GND
28	GND	UPHY_RX17_N	GND	UPHY_RX16_P	GND	UPHY_REFCLK2_P
29	GND	UPHY_RX17_P	GND	UPHY_RX16_N	GND	UPHY_REFCLK2_N
30	UPHY_RX19_P	GND	UPHY_RX18_N	GND	UPHY_REFCLK0_P	GND
31	UPHY_RX19_N	GND	UPHY_RX18_P	GND	UPHY_REFCLK0_N	GND
32	GND	UPHY_RX21_N	GND	UPHY_RX22_N	GND	UPHY_REFCLK3_P
33	GND	UPHY_RX21_P	GND	UPHY_RX22_P	GND	UPHY_REFCLK3_N
34	UPHY_RX23_P	GND	UPHY_RX20_P	GND	RSVD	GND
35	UPHY_RX23_N	GND	UPHY_RX20_N	GND	RSVD	GND
36	GND	PEX_C7_RST_N	GND	RSVD	GND	RSVD
37	GND	PEX_C7_CLKREQ_N	GND	PMIC_BBATT	GND	RSVD
38	PEX_C8_CLKREQ_N	GND	UPHY_REFCLK4_N	GND	CSI0_D1_N	GND
39	PEX_C8_RST_N	GND	UPHY_REFCLK4_P	GND	CSI0_D1_P	GND
40	GND	RSVD	GND	RSVD	GND	RSVD
41	CSI2_D0_P	GND	CSI2_D1_N	GND	CSI0_D0_N	GND
42	CSI2_D0_N	CSI2_CLK_N	CSI2_D1_P	CSI5_D0_P	CSI0_D0_P	CSI0_CLK_N
43	GND	CSI2_CLK_P	GND	CSI5_D0_N	GND	CSI0_CLK_P
44	CSI7_D0_P	GND	CSI5_CLK_P	GND	CSI3_D0_N	GND
45	CSI7_D0_N	CSI7_CLK_P	CSI5_CLK_N	CSI5_D1_N	CSI3_D0_P	CSI3_CLK_N
46	GND	CSI7_CLK_N	GND	CSI5_D1_P	GND	CSI3_CLK_P
47	GPIO38	GND	CSI7_D1_P	GND	CSI4_D1_P	GND
48	GPIO37	RSVD	CSI7_D1_N	PEX_CLK6_N	CSI4_D1_N	CSI4_CLK_P
49	GND	RSVD	GND	PEX_CLK6_P	GND	CSI4_CLK_N
50	HDMI_DP2_TX2_N	GND	HDMI_DP2_TX3_N	GND	RSVD	GND
51	HDMI_DP2_TX2_P	HDMI_DP2_TX1_P	HDMI_DP2_TX3_P	HDMI_DP2_TX0_P	RSVD	DP0_AUX_CH_N
52	GND	HDMI_DP2_TX1_N	GND	HDMI_DP2_TX0_N	GND	DP0_AUX_CH_P

	A	B	C	D	E	F
53	I2C5_CLK	GND	I2C5_DAT	GND	I2C3_DAT	I2C3_CLK
54	GPIO17	WDT_RESET_OUT_N	GPIO33	GPIO03	FAN_TACH	GPIO22
55	GPIO34	GPIO30	GPIO18	SPI1_MOSI	SPI1_CS0_N	SPI3_CLK
56	SPI1_MISO	SPI1_CS1_N	UART2_RX	SPI3_MISO	SPI3_CS1_N	GPIO36
57	UART2_CTS	GND	SPI3_CS0_N	GND	GND	GND
58	GPIO20	GPIO21	UART2_TX	JTAG_TDO	JTAG_TMS	CAN0_DIN
59	GPIO05	GPIO04	I2S3_SCLK	CAN0_DOUT	GPIO06	GPIO07
60	JTAG_TCK	JTAG_TDI	I2S3_FS	SPI2_CS0_N	I2C4_DAT	SPI2_MOSI
61	SYSTEM_OC_N	CAN1_DIN	GPIO09	I2C4_CLK	SPI2_CLK	VCOMP_ALERT_N
62	GPIO10	GPIO08	GND	SPI2_MISO	GND	GND
63	GND	SYS_VIN_HV	SYS_VIN_HV	GND	SYS_VIN_HV	SYS_VIN_HV
64			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV
65			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV

Legend	Ground	Power	RSVD – Must be left unconnected unless otherwise directed.	Different functionality between JAO and JAOi	No pins at that location

Table 2-3. Connector Pinout Matrix Part 2: Columns G-L

	G	H	J	K	L
01	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		
02	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		
03	GND	SYS_VIN_HV	GND	SYS_VIN_HV	GND
04	I2S2_CLK	GND	GPIO01	GND	UART4_RTS
05	RGMII_TD1	ENET_RST_N	ENET_INT	I2C1_CLK	UART4_TX
06	RGMII_TD3	RGMII_RD2	RGMII_TD0	RGMII_RD1	GPIO02
07	GPIO13	GND	RGMII_TD2	RGMII_TX_CTL	GND
08	PEX_C4_CLKREQ_N	I2S1_SDIN	GND	GND	I2C1_DAT
09	GND	MCLK01	PEX_C4_RST_N	PEX_C3_RST_N	GPIO28
10	USB3_N	PEX_C5_RST_N	PEX_C3_CLKREQ_N	PEX_C2_RST_N	FORCE_RECOVERY_N
11	USB3_P	GND	PEX_C2_CLKREQ_N	GND	SLEEP_REQ_N
12	GND	UPHY_TX11_P	GND	UPHY_TX10_N	GND
13	GND	UPHY_TX11_N	GND	UPHY_TX10_P	GND
14	UPHY_TX9_N	GND	UPHY_TX8_P	GND	I2S1_CLK
15	UPHY_TX9_P	GND	UPHY_TX8_N	GND	GPIO14
16	GND	UPHY_TX7_P	GND	UPHY_TX6_N	GND
17	GND	UPHY_TX7_N	GND	UPHY_TX6_P	GND
18	UPHY_TX5_N	GND	UPHY_TX4_P	GND	PEX_C6_RST_N
19	UPHY_TX5_P	GND	UPHY_TX4_N	GND	PEX_C6_CLKREQ_N
20	GND	UPHY_TX3_P	GND	UPHY_TX2_N	GND
21	GND	UPHY_TX3_N	GND	UPHY_TX2_P	GND
22	UPHY_TX1_N	GND	UPHY_TX0_P	GND	SYS_VIN_MV
23	UPHY_TX1_P	GND	UPHY_TX0_N	GND	SYS_VIN_MV
24	GND	UPHY_TX12_P	GND	UPHY_TX13_N	GND
25	GND	UPHY_TX12_N	GND	UPHY_TX13_P	GND
26	UPHY_TX14_N	GND	UPHY_TX15_P	GND	SYS_VIN_MV
27	UPHY_TX14_P	GND	UPHY_TX15_N	GND	SYS_VIN_MV
28	GND	UPHY_TX16_P	GND	UPHY_TX17_N	GND
29	GND	UPHY_TX16_N	GND	UPHY_TX17_P	GND
30	UPHY_TX18_N	GND	UPHY_TX19_P	GND	SYS_VIN_MV
31	UPHY_TX18_P	GND	UPHY_TX19_N	GND	SYS_VIN_MV
32	GND	UPHY_TX23_P	GND	UPHY_TX20_P	GND

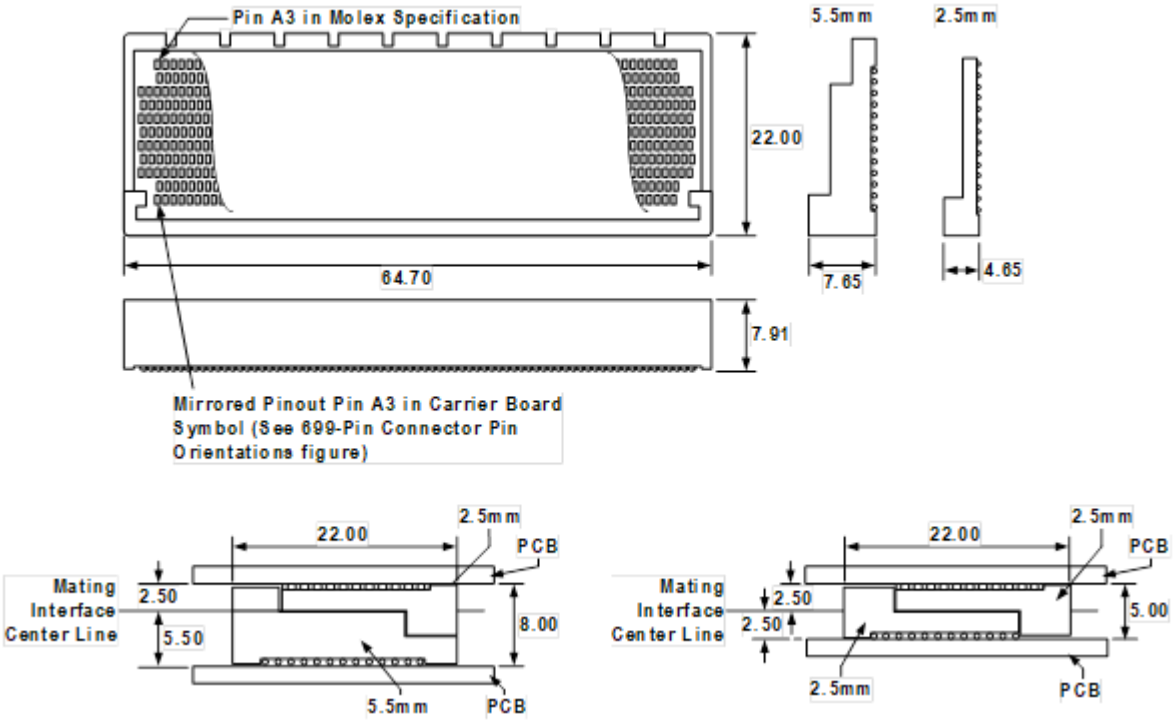
	G	H	J	K	L
33	GND	UPHY_TX23_N	GND	UPHY_TX20_N	GND
34	UPHY_TX21_N	GND	UPHY_TX22_N	GND	SYS_VIN_MV
35	UPHY_TX21_P	GND	UPHY_TX22_P	GND	SYS_VIN_MV
36	GND	RSVD	GND	RSVD	GND
37	GND	RSVD	GND	RSVD	GND
38	RSVD	GND	RSVD	GND	SYS_VIN_MV
39	RSVD	GND	RSVD	GND	SYS_VIN_MV
40	GND	MID1	GND	MID0	GND
41	CSI1_D0_P	GND	CSI1_D1_P	GND	RSVD
42	CSI1_D0_N	CSI1_CLK_N	CSI1_D1_N	GND	RSVD
43	GND	CSI1_CLK_P	GND	CSI6_D0_N	GND
44	CSI3_D1_P	GND	CSI6_CLK_P	CSI6_D0_P	RSVD
45	CSI3_D1_N	CSI6_D1_N	CSI6_CLK_N	GND	RSVD
46	GND	CSI6_D1_P	GND	RSVD	GND
47	CSI4_D0_N	GND	RSVD	RSVD	RSVD
48	CSI4_D0_P	RSVD	RSVD	GND	UART4_RX
49	GND	RSVD	GND	GPIO25	UART4_CTS
50	RSVD	GND	HDMI_CEC	DP2_HPD	GPIO35
51	RSVD	GPIO26	GPIO24	DP1_HPD	UART1_RTS
52	GND	GPIO27	DP1_AUX_CH_P	DP0_HPD	MODULE_SHDN_N
53	DP2_AUX_CH_P	MCLK03	DP1_AUX_CH_N	UART1_TX	RSVD for JAO Tie to 3.3V for JAOi
54	DP2_AUX_CH_N	UART1_CTS	MCLK02	UART1_RX	MODULE_POWER_ON
55	GPIO23	MCLK04	GPIO32	GND	VDDIN_PWR_BAD_N
56	SPI3_MOSI	GND	GND	GPIO19	THERM_ALERT_N
57	GND	UART5_CTS	SPI1_CLK	PWM01	MCLK05
58	UART2_RTS	UART5_RX	UART5_TX	UART5_RTS	PERIPHERAL_RESET_N
59	RSVD	NVJTAG_SEL	I2S3_DIN	I2S3_DOUT	RSVD
60	NVDBG_SEL	GPIO31	MODULE_SLEEP_N	UART3_RX_DEBUG	SYS_RESET_N
61	JTAG_TRST_N	CAN1_DOUT	I2C2_CLK	I2C2_DAT	POWER_BTN_N
62	GND	UART3_TX_DEBUG	RSVD Connect to GND through 0Ω resistor	FAN_PWM	CARRIER_POWER_ON
63	SYS_VIN_HV	GND	SYS_VIN_HV	GND	PRSNT1/GND_LOOP_1
64	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		
65	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		

Legend	Ground	Power	RSVD – Must be left unconnected unless otherwise directed.	Different functionality between JAO and JAOi	No pins at that location

Chapter 3. Main Connector Details

The main 699-pin connector on the Orin module is from the Molex Mirror Mezz family. See the *Jetson AGX Orin Series Supported Components List* for compatible module connectors to use on the carrier board. Refer to the Molex Mirror Mezz connector specification for details.

Figure 3-1. 699-pin Connector Dimensions



Notes: Various documents related to the Molex Mirror Mezz connector can be found at:

Mirror Mezz Connectors - Molex

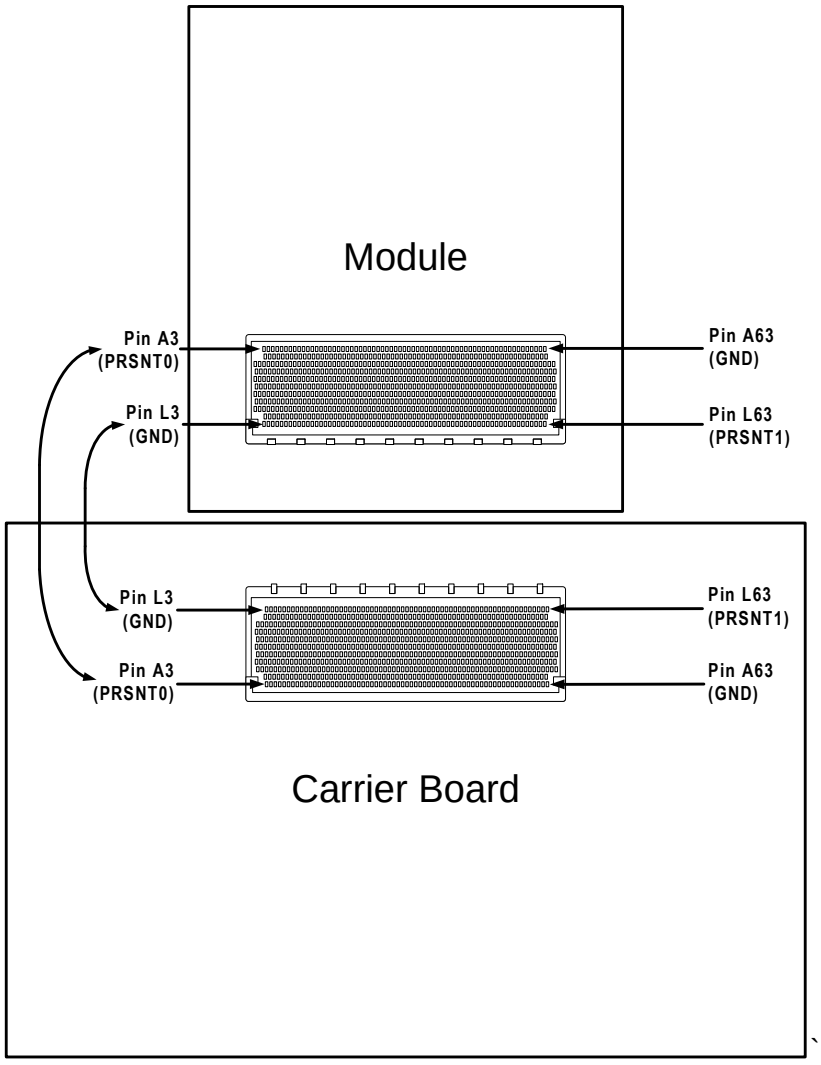
The *Molex Application Guide* for Mirror Mezz™ which includes details for connector mounting can be found at: https://www.molex.com/pdm_docs/as/2028280001-AS-000.pdf

3.1 Connector Pin Orientations

The symbol pinout for the 699-pin connector on the carrier board is mirrored such that the pin numbers match when the module and carrier board connectors are mated (see Figure 3-2). The orientation shown matches the carrier board in the upright position as well as the layout file.

CAUTION: Note that the 699-pin connector pinout on the carrier board is a mirror image of the Molex pinout. Designers should verify the pinout of their designs against the Jetson AGX Orin reference layout.

Figure 3-2. 699-pin Connector Pin Orientation



3.2 Module to Carrier Board Standoff

The spacing between the module PCB and the carrier board PCB are shown in Figure 3-3 and Figure 3-4 to illustrate the following two cases:

- 5.5 mm connector on the carrier board (8 mm nominal spacing).
- 2.5 mm connector (5 mm nominal spacing).

The standoffs to support the module are located between the carrier board and the bottom plate.

Figure 3-3. 5.5 mm Height on Carrier Board

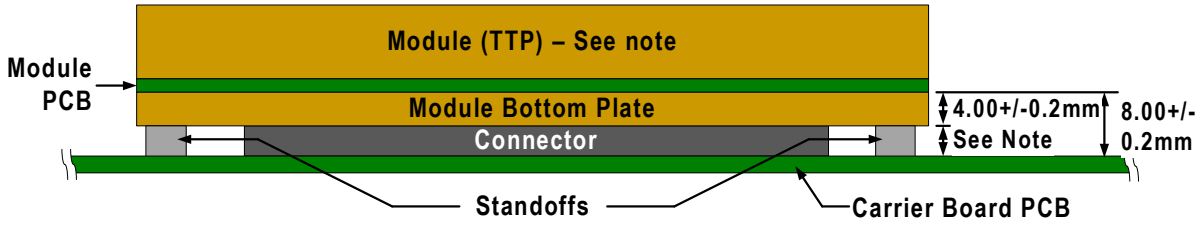
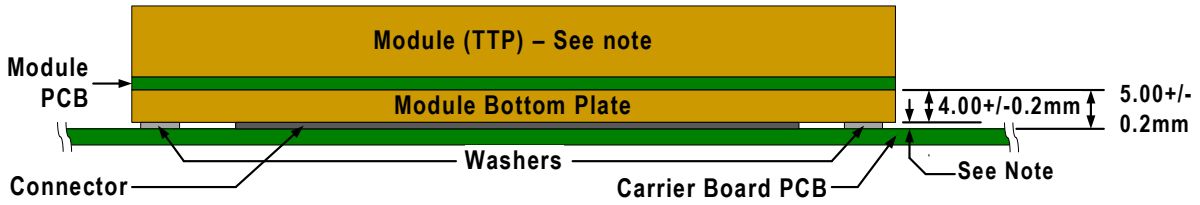


Figure 3-4. 2.5 mm Height on Carrier Board



Notes:

See Section 3.3 on recommendations for standoff heights.

If the 2.5 mm height connector is used, there can be no components under the module on the carrier board due to the extremely limited clearance.

3.3 Module to Carrier Board Standoff Height Recommendations

Standoffs and spacers are required between the module bottom plate and the carrier board. The height should be chosen to meet the connector board-to-board spacing requirements and accommodate the tolerances in the bottom plate and the standoff itself. If the standoff is too short, the carrier board PCB may warp as the mounting screws are tightened. If too tall, the connectors will not mate fully. The two cases (5.5 mm and 2.5 mm connector on carrier board) are described in this section and are accompanied with tables that show the possible permutations of tolerances of the bottom plate and spacers. The platform designer can determine if a different height would be more appropriate but should consider both the PCB warpage (standoff height too short) and connector contact overlap length to find the best balance.

The following examples are based on Molex parts using spacer heights and spacer tolerances to produce a workable solution.

5.5 mm height – 8.00+/-0.15 mm board to board spacing case

For this case, a standoff height of 4.2 mm is used. This is based on a standoff with ±0.13 mm height tolerance. The tolerance for the bottom plate is ±0.1 mm and ±0.1 mm for the solder balls between the bottom plate and the module PCB. Table 3-1 shows example calculations using the connector board spacing, module bottom plate height and example standoff height with tolerances mentioned.

Table 3-1. Standoff Height Calculations for 5.5 mm Height Connector Case

Board to Board Spacing (mm)	Bottom Plate Height (mm)	Board to Bottom Plate Gap (mm)	Standoff Height (mm)	Space Beyond Ideal Mating Spec. (mm)
8	3.8	4.2	4.07	-0.13
8	3.8	4.2	4.33	0.13
8	4.2	3.8	4.07	0.27
8	4.2	3.8	4.33	0.53
Margin to -0.15 mm Conn. Spec.				0.02
Nominal connector sweep range				1.5
Worst case remaining sweep/contact (mm)				0.97

Notes:

1. Positive values mean no PCB warpage but less sweep. Negative values can result in PCB warpage.
2. The mating connector height tolerance comes from the Molex connector specification.
3. The connector contact sweep range can be found on the Molex website in the Mirror Mezz area.
4. The module bottom plate height/tolerance can be found in the Jetson AGX *Orin Data Sheet*.

2.5 mm height – 5.00+/-0.15 mm board to board spacing case

For this case, a standoff height of 1.2 mm is used. This is based on a standoff with ±0.13 mm height tolerance. The tolerance for the bottom plate is ±0.1 mm and ±0.1 mm for the solder balls between the bottom plate and the module PCB. Table 3-2 shows example calculations using the connector board spacing, module bottom plate height and example standoff height with tolerances mentioned.

Table 3-2. Standoff Height Calculations for 2.5 mm Height Connector Case

Board to Board Spacing (mm)	Bottom Plate Height (mm)	Board to Bottom Plate Gap (mm)	Standoff Height (mm)	Space Beyond Ideal Mating Spec. (mm)
5	3.8	1.2	1.07	-0.13
5	3.8	1.2	1.33	0.13
5	4.2	0.8	1.07	0.27
5	4.2	0.8	1.33	0.53
Margin to -0.15mm Conn. Spec.				0.02
Nominal connector sweep range				1.5
Worst case remaining sweep/contact (mm)				0.97

Notes:

1. Positive values mean no PCB warpage but less sweep. Negative values can result in PCB warpage.
2. See additional notes in the "Notes" section of Table 3-1.

3.4 Module Installation and Removal

To install the Orin module correctly, follow the following sequence and mounting hardware instructions:

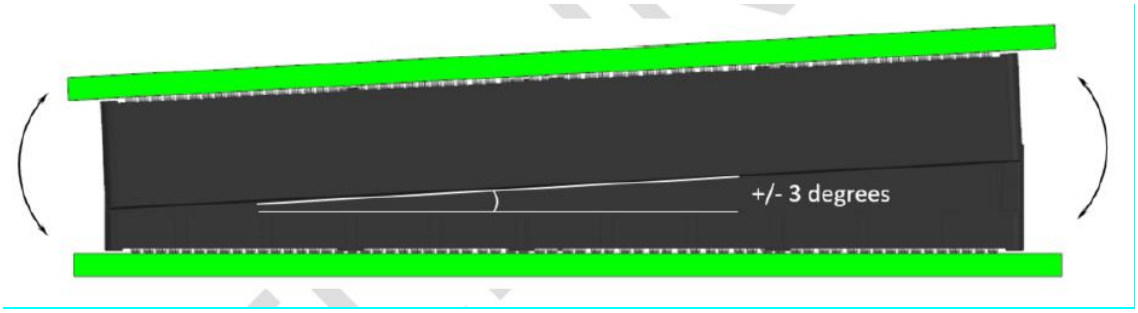
1. Connectors should be parallel with respect to each other during mating.
2. Use a smooth motion during mating (no mechanical shock, knocking, hammering).
3. The top and bottom PCB are to be bolted to enhance reliability.
4. Secure with M3 screws (4x) from the top of the module. Torque the screws to 4.5 in-lbf.

If a fixture is used to do the mating, then that fixture should hold the mating connectors parallel to within ± 2 degrees. Also, the fixture should allow the connectors to become parallel as the mating process progresses.

To remove the Orin module correctly, follow the following sequence and mounting hardware instructions:

1. The PCB design needs to have enough finger reachability and space required to hold the board for un-mating.
2. Remove mounting screws (4x) from the top of the module.
3. Rock the top board a few times, no more than ± 3 degrees, to gradually disengage the connectors.

Figure 3-5. Module Removal



Chapter 4. Reference Design Considerations

The Jetson AGX Orin Developer Kit Carrier Board design files are provided as a reference design. This chapter describes details necessary for designers to know to replicate certain features if desired. In addition, aspects of the design that are specific to the NVIDIA developer kit usage but not useful or supported on a custom carrier board are also identified.

Most of the features implemented on the Jetson AGX Orin Developer Kit carrier board design can be duplicated by copying the connections from the P3737 carrier board reference design. These following listed features have aspects that would require additional information.

- Button Power MCU: The developer kit carrier board implements a button power MCU (EFM8SB10F2G – U79 on the P3737 carrier board). This device is programmed with firmware that is available on the Jetson Download Center. The posting is titled *NVIDIA Jetson AGX Orin, Jetson Orin Nano, Jetson AGX Xavier, and Jetson Xavier NX Power Button Supervisor Firmware*. The connections used on the reference design must be followed exactly and the firmware provided must be used to ensure correct functionality.
- USB Type C PD Controller: Designs that intend to follow the NVIDIA carrier board design and include the Type C PD Controller (CYPD4226 - U513 on the P3737 carrier board) must replicate the circuitry on the latest carrier board exactly. The firmware binary is used to program the Cypress CYPD4226 controller and is available on the Jetson Download Center. The posting is titled *Cypress Firmware Binary for USB Type-C PD controller (CYPD4226)*. The customer should get the flashing instructions from Cypress. No support or source code is provided for this firmware. If modifications or source code is required, Cypress should be contacted directly for support. This firmware binary is released under the L4T firmware EULA.

The following list is the Jetson AGX Orin Developer Kit carrier board features that should not be copied as they are not required or useful for a custom carrier board design. They will not be supported by NVIDIA.

- The ID EEPROM (P3737 – U501) is a feature that is used for NVIDIA internal purposes, but not useful on a custom design. A similar function may be desired for a custom design, but the NVIDIA software will not interact with these devices and the I2C address used by the developer kit carrier board ID EEPROM on the I2C1 interface (7'h56) should be avoided.
- Debug MCU (ATSAMD21G16B0AU – U136), circuit, and associated USB Micro B connector (J26): These features are used at NVIDIA for internal debugging and development purposes. These are not required, and support will not be provided if implemented. Designers have the option to implement something similar on their custom carrier boards but should develop their own circuit to meet their needs.

Chapter 5. Power

This chapter describes the power specifications for the Orin module.

> **!** CAUTION: The Jetson AGX Orin module is not hot-pluggable. Before installing or removing the module, the main power supplies (SYS_VIN_HV, SYS_VIN_MV, and SYS_VIN_SV (JAOi only) if implemented) must be disconnected and the power rails allowed to discharge to <0.6V.

Table 5-1. Power and System Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
Note 1	SYS_VIN_HV	–	System Voltage Input - High	Input	Power: 7V to 20V
Note 2	SYS_VIN_MV	–	System Voltage Input - Medium	Input	Power: 5.0V
L53	RSVD for JAO SYS_VIN_SV for JAOi	–	JAO: Unused JAOi: Must be tied to 3.3V. See power sequencing for timing.	NA Input	NA Power: 3.3V
D37	PMIC_BBATT	–	Real-Time Clock: Optionally used to provide back-up power for RTC in the Power Sequencer. Connects to Lithium Cell or similar power source which provides power to RTC when system is disconnected from power. Note that unlike previous Jetson modules, this RTC back-up pin is input only. Rechargeable cells or super capacitors are not supported.	Input	Power: 1.85V to 5.5V
L60	SYS_RESET_N	–	System Reset: Driven by power sequencer reset during power-on. Can be asserted by the carrier board to reset the SoC, Boot device, etc., but not the power sequencer. A 10kΩ pull-up to 1.8V is present on the module.	Bidir	Open Drain, 1.8V
L55	VDDIN_PWR_BAD_N	–	VDD_IN Power Bad: Carrier board indication to module that VDD_IN power is not valid. Carrier board should stop asserting this signal and allow on-module pull-up to bring high only when HV/MV are stable and have have reached required voltage levels. This prevents SoC from powering up until the main input supply voltages are stable. Can also be driven by module if critical condition makes this necessary. 10kΩ pull-up to 5V on the module.	Bidir	Open-drain – 5.0V

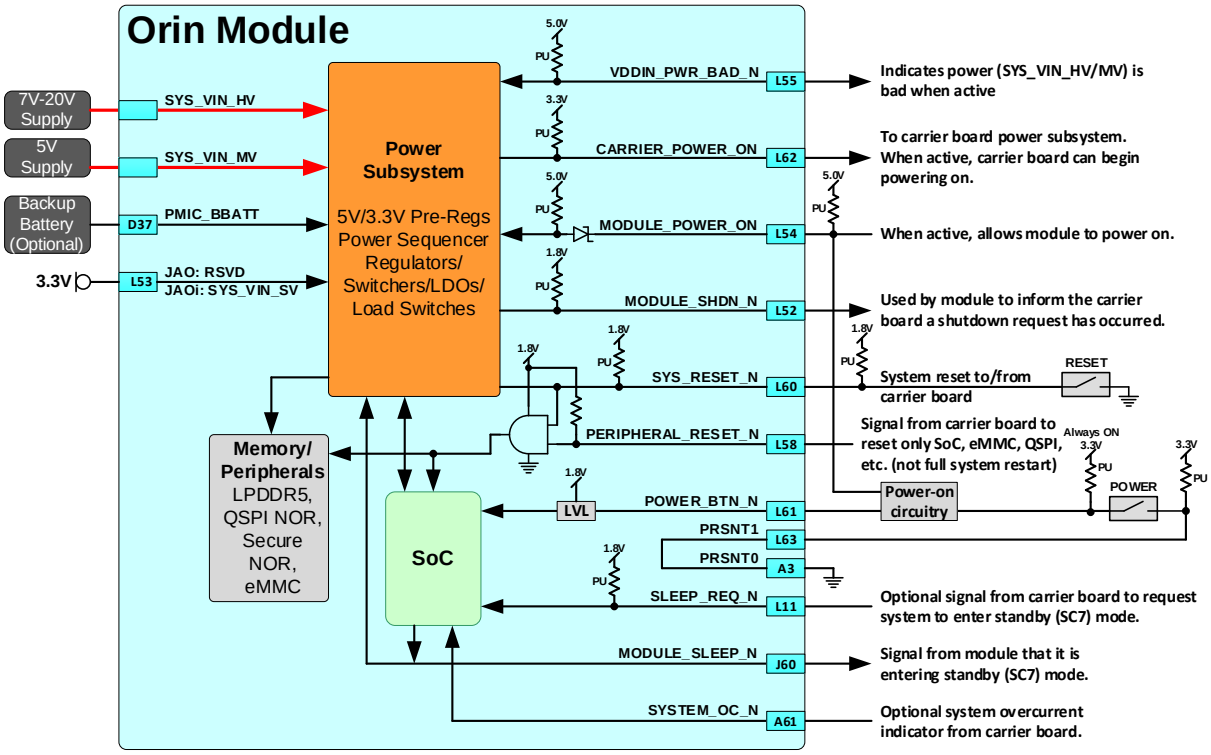
Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
L54	MODULE_ POWER_ON	–	Module Power On: Signal asserted to the module to start power-on sequence. This signal should be driven low by the carrier board initially and then driven high when the module is to be powered on.	Input	CMOS - 5.0V
L62	CARRIER_ POWER_ON	–	Carrier Power On: Used as part of the power up sequence. When asserted, it is safe for the carrier board to power up. 10kΩ pull-up to 3.3V on module.	Output	N/A
L61	POWER_BTN_N	GP04	Power Button: Can be configured by software to be used to power system off or enter and exit sleep mode (SC7). Level shifter between module pin (3.3V) and SoC pin (1.8V) on module.	Bidir	Open-drain, 3.3V
L58	PERIPHERAL_ RESET_N	–	Peripheral Reset: Driven from carrier board and AND'd with SYS_RESET_N to drive the Orin SF_SYS_RST_N pin. When PERIPHERAL_RESET_N is asserted, the SoC, eMMC, & QSPI are reset (not Power Sequencer). 100kΩ pull-up to 1.8V on the module.	Input	CMOS – 1.8V
L10	FORCE_ RECOVERY_N	GP107_ RECOVERY0_ STRAP	Force Recovery strap pin: Held low when SYS_RESET_N goes inactive (power-on or reset button press) to enter force recovery mode.	Input	CMOS – 1.8V
L11	SLEEP_REQ_N	GP109	Sleep Request: Requests module to enter sleep mode (SC7 state). A 10kΩ pull-up to 1.8V is present on the module.	Input	CMOS – 1.8V
J60	MODULE_SLEEP_N	SF_PWR_ SOC_EN	Sleep Acknowledge: Indicates module is in sleep mode (SC7 state).	Bidir	CMOS – 1.8V
B54	WDT_RESET_OUT_N	GP63	Watch-Dog Timer Reset output.	Bidir	CMOS – 1.8V
F61	VCOMP_ALERT_N	GP01	Supports either GPIO operation or SoC Thermal Over-current alert #1.	Bidir	Open-drain, 1.8V (note 3)
L56	THERM_ALERT_N	GP108	ALERT*/THERM2 from Temp Sensor on module	Output	Open-drain, 1.8V
A61	SYSTEM_OC_N	GP03	System Over-current Thermal warning	Input	CMOS, 1.8V (note 3)
L52	MODULE_SHDN_N	GP67	Module Shutdown Request. Used to inform carrier board that a shutdown request has occurred on-module (either software shutdown via SoC, or thermal shutdown). A 10kΩ pull-up to 1.8V is present on the module.	Output	CMOS – 1.8V (note 3)
A3	PRSNT0	–	Present #[1:0]: Tied together on module. Used to detect when module is connected to the carrier board. Can be used to keep carrier board from powering the module until the module is installed fully in the carrier board. Tied to GND on carrier board if implemented to match reference design.	N/A	N/A
L63	PRSNT1	–	Tied to one side of power button on carrier board.		
K40	MID0	–	Module ID #0	Not connected	N/A

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
H40	MID1	–	Module ID #1	Tied to GND	N/A

Notes:

1. SYS_VIN_HV pin #s: C65, D65, E65, F65, G65, H65, J65, C64, D64, E64, F64, G64, H64, J64, B63, C63, E63, F63, G63, J63, B3, D3, F3, H3, K3, C2, D2, E2, F2, G2, H2, J2, C1, D1, E1, F1, G1, H1, J1.
2. SYS_VIN_MV pin #s: L39, L38, L35, L34, L31, L30, L27, L26, L23, L22.
3. These pins are 3.3V tolerant and back-drive capable to 1.8V.
4. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.

Figure 5-1. Power Block Diagram



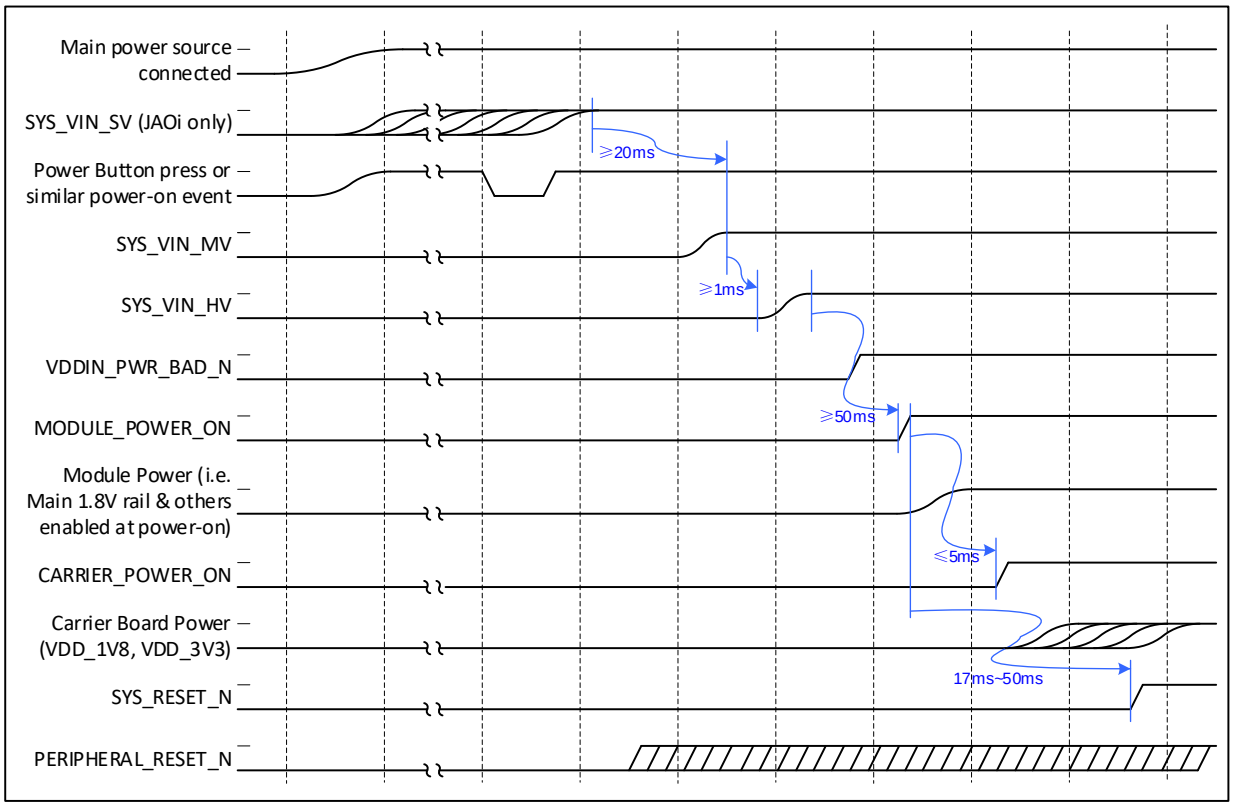
5.1 Power Sequencing

5.1.1 Power On Sequence

The basic power on sequencing requirements is as follows:

- The main power source for the system is applied. The SYS_VIN_SV (JAOi only), SYS_VIN_HV, and SYS_VIN_MV are derived from this power source. SYS_VIN_SV (JAOi only) must be powered up first or may have remained powered from previous power cycle. Optionally, SYS_VIN_SV, SYS_VIN_HV, and SYS_VIN_MV supplies can be gated and only enabled to the module when a signal (such as VIN_PWR_ON) is enabled. This can help avoid damage if the module is inserted when main power is on.
- VDDIN_PWR_BAD_N will stay active (low) until SYS_VIN_MV is valid (and not gated).
- MODULE_POWER_ON can be set active (high) once VDDIN_PWR_BAD_N is inactive (high).
- As the module powers on, one of the last supplies is the 3.3V supply always-on supply. CARRIER_POWER_ON is pulled up to the powergood pin of the 3.3V supply. Once this signal is active (high), the carrier board supplies associated with the module (1.8V, 3.3V) can power on.
- SYS_RESET_N is driven by the power sequencer on the module during power-on. It does not need to be controlled by the carrier board. If the carrier board supplies required for powering on require additional time, the PERIPHERAL_RESET_N signal can be held low. This will keep the SoC and other boot devices in reset.

Figure 5-2. Power On Sequence (Power Button Case)



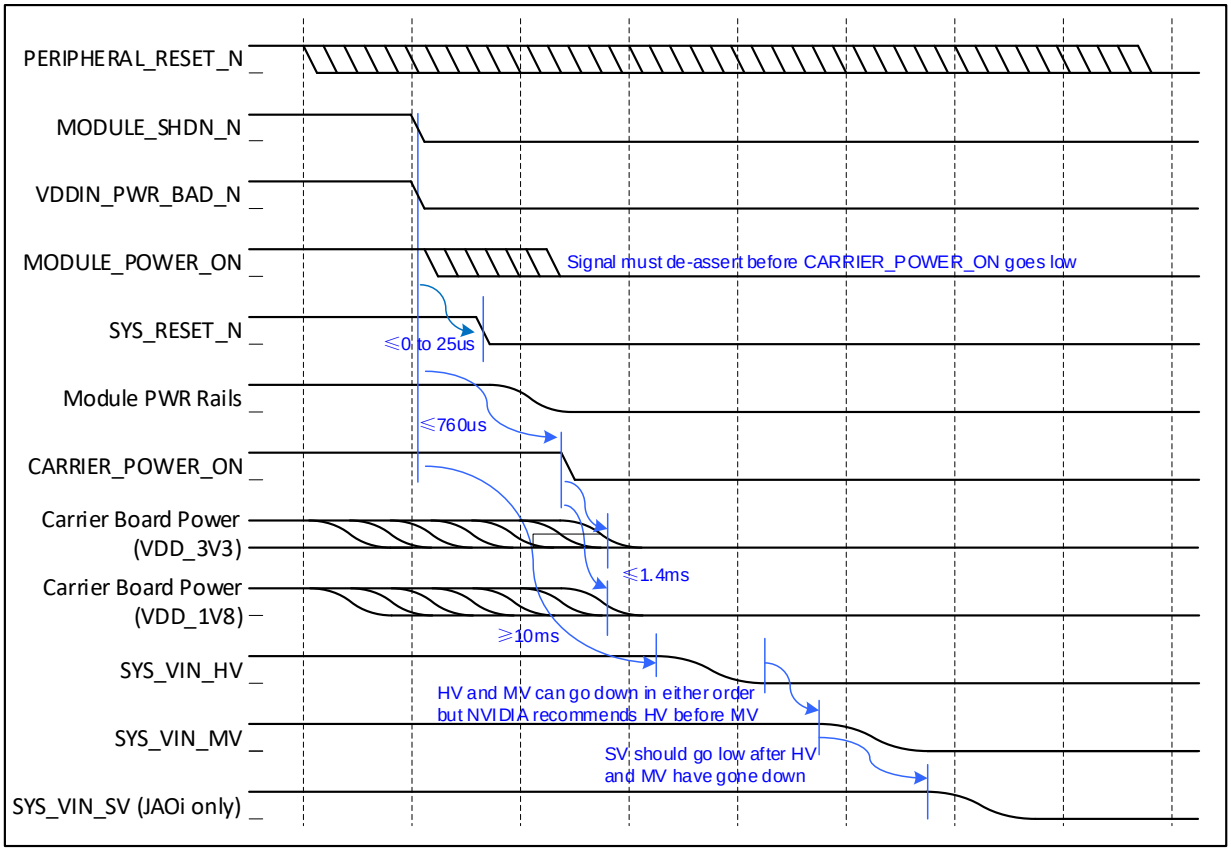
Notes:

1. PERIPHERAL_RESET_N is optionally kept High during the power-up sequence. If Carrier Board Power in not up yet by the time SYS_RESET_N is de-asserted, PERIPHERAL_RESET_N must be held Low until the carrier board is ready to bring Orin out of RESET.
2. MODULE_POWER_ON must be driven low by the carrier board initially before driving it high to power on the module during the power-on sequence.

5.1.2 User Initiated SW Shutdown

1. MODULE_SHDN_N is the first signal to assert low.
2. VDDIN_PWR_BAD_N is tied to MODULE_SHDN_N as such asserts low at the same time.
3. MODULE_POWER_ON signal should go low almost immediately. With the button MCU solution used on the reference design, MODULE_POWER_ON will go low after a propagation delay/ MCU response time as VDDIN_PWR_BAD_N notifies the Button MCU to go to shutdown state.
4. The power sequencer on the module starts power down sequence from the moment MODULE_SHDN_N goes low.

Figure 5-3. Power Down Sequence – User Initiated – SW Shutdown Case



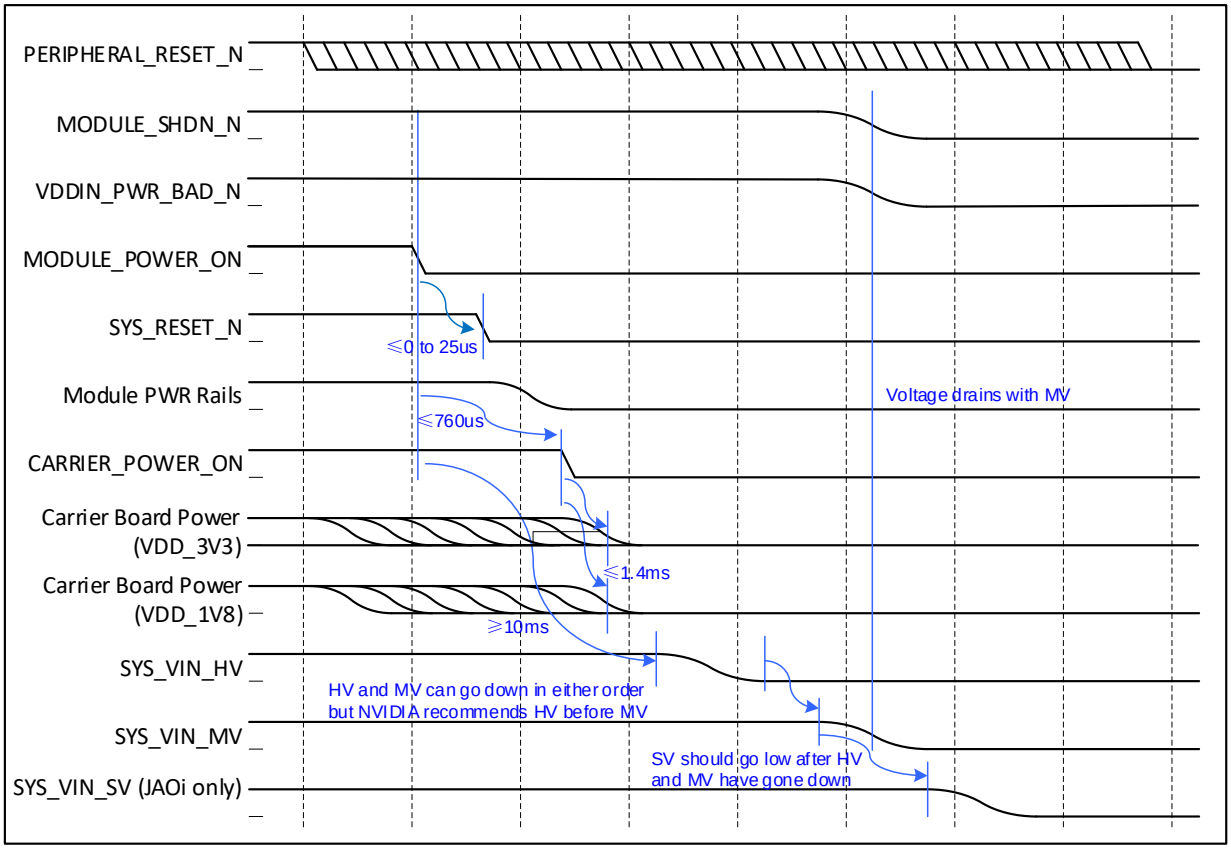
Note:

1. Once CARRIER_POWER_ON is de-asserted by the module, back drive into Orin I/O from the carrier board must be eliminated by this point.
2. SYS_VIN_MV must go below 100 mV before system can be powered on again.

5.1.3 User initiated Button Press Shutdown

1. MODULE_SHDN_N and VDDIN_PWR_BAD_N do not play a role in this power down sequence. They drain with the MV rail going down at the end.
2. MODULE_POWER_ON signal goes low assuming a solution similar to the button MCU circuit used on the reference design is used and the user holds the Power Button for X-amount of time (see the 5.3.2 Power Button Supervisor MCU section).
3. The power sequencer on the module starts the power down sequence from the moment MODULE_POWER_ON goes low.

Figure 5-4. Power Down Sequence – Button Press Shutdown Case



Note:

1. Once CARRIER_POWER_ON is de-asserted by the module, back drive into Orin I/O from the carrier board must be eliminated by this point.
2. SYS_VIN_MV must go below 100 mV before system can be powered on again.

5.1.4 Shutdown Due to an Event

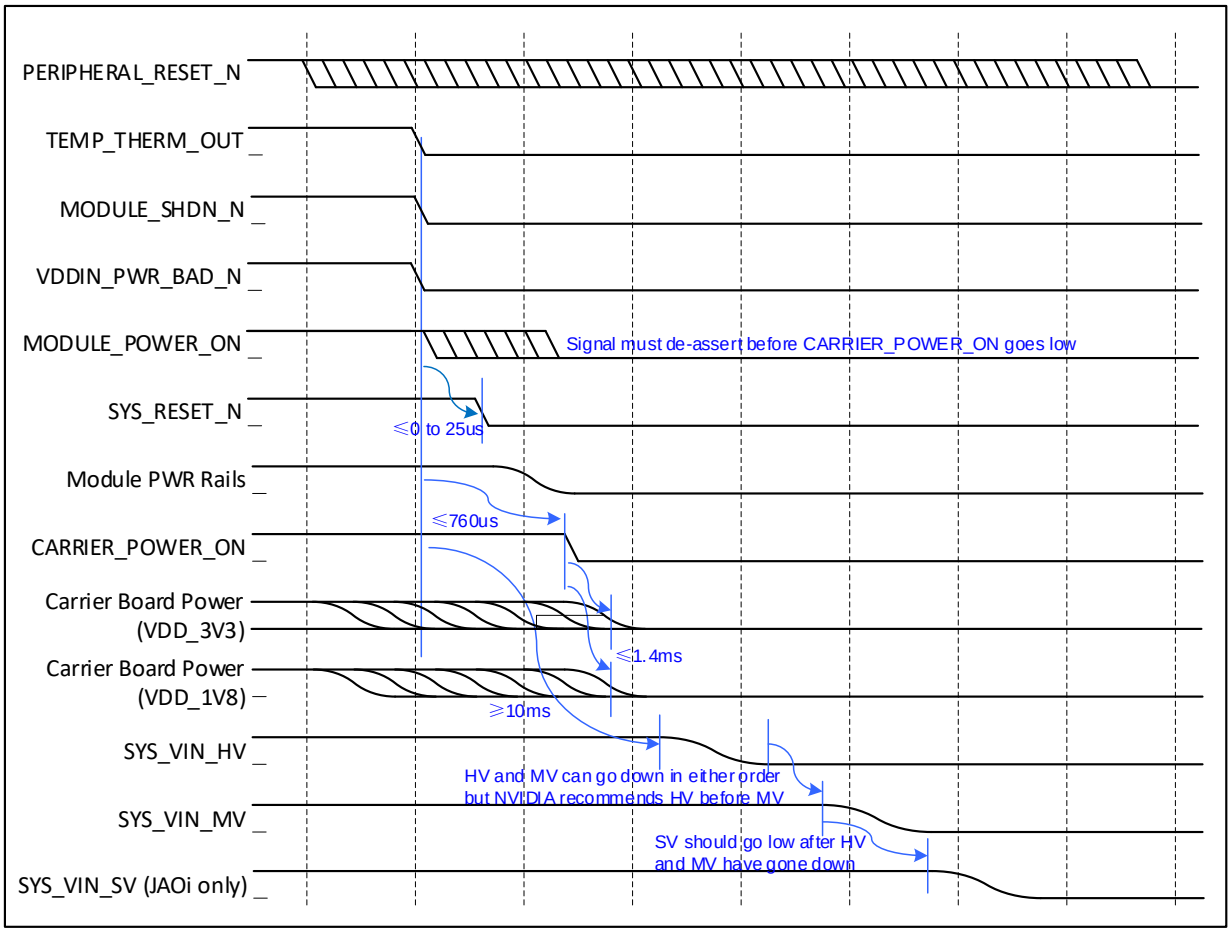
1. VDDIN_PWR_BAD_N, MODULE_SHDN_N and TEMP_THERM signals are essentially all tied together. If any of these signals go down, then all signals go down together, initiating an event based shutdown.
2. The description of the above 4 signals and their respective triggers is as follows:

- VDDIN_PWR_BAD_N = This signal will come from carrier board. Voltage monitoring will pull this signal low if goes below a threshold initiating a shutdown. This signal should go to a circuit on the carrier board that will simultaneously pull MODULE_POWER_ON low so the logic on module and carrier board is same (a state of shutdown). This is implemented in the Power Button MCU circuit on the reference design.
- MODULE_SHDN_N = MODULE_SHDN_N is a way for the module to communicate both to power sequencer on the module and to the carrier board that it needs to shut down right away (either due to module thermal sensor or SW shutdown). The reference schematic

direction of input to Orin is erroneous, it should be output. This signal will simultaneously tell the power sequencer on the module to shutdown and the carrier board should have matching logic to turn off MODULE_POWER_ON.

- TEMP_THERM = Thermal sensor monitoring critical temperature, initiates a thermal shutdown - Same as above cases.

Figure 5-5. Power Down Sequence – Shutdown Due to an Event Case



Notes (see Figure 5-5):

1. Once CARRIER_POWER_ON is de-asserted by the module, back drive into Orin I/O from the carrier board must be eliminated by this point.
2. SYS_VIN_MV must go below 100 mV before system can be powered on again.
3. If the main power rails (SYS_VIN_HV/MV) are not powered off, it is possible for the system to power on again depending on the state of the signals. If the system was powered down due to a shutdown condition that is cleared, the system may power back on. Unless this is desired, a means of keeping the module powered off should be provided. One way is to latch the state of CARRIER_POWER_ON when it goes from high to low (module powered off) and using this to keep MODULE_POWER_ON inactive (low).

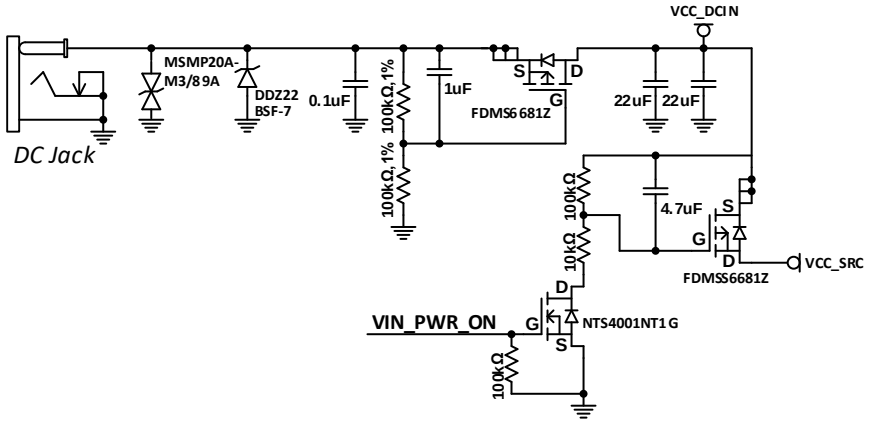
5.2 SYS_VIN_HV Input

The Jetson AGX Orin Developer Kit carrier board allows the main system power to be supplied either by one of the USB Type C connectors or a DC power jack. The details for implementing Type C for power, and so on, can be found in the P3737 reference schematics. If a design only requires a simple DC power jack, the circuit in Figure 5-6 can be used.

Note: Designs that intend to follow the NVIDIA carrier board design and include the Type C PD Controller (CYPD4226 - U513 on NVIDIA carrier board) must replicate the circuitry on the latest P3737 carrier board exactly. NVIDIA will provide the binary and the customer should get the flashing instructions from Cypress.

The example shown in Figure 5-6 shows the main system power being supplied to the carrier board by a DC power jack. This circuit is a simplified example based on the carrier board reference design.

Figure 5-6. Simplified DC Jack Power Connections



Note: Designs which implement an eFUSE or current limiting device on the input power rail of the module should select a part that DOES NOT limit reverse current.

5.3 Power-On

This section provides examples for powering on the Orin module.

- Auto power-on requirements
- Power button supervisor MCU circuit

5.3.1 Auto Power-on

If the system does not require a power button or equivalent, and should power on when the main power source is connected, the following requirements should be met:

- SYS_VIN_HV, SYS_VIN_MV, and SYS_VIN_SV (JAOi only) should be powered on. These can be optionally gated and a signal used to enable them when the module is detected mounted correctly using PRSNT[1:0].
- VDDIN_PWR_BAD_N should be de-asserted (high) once the SYS_VIN_HV/MV supplies are enabled and stable.
- MODULE_POWER_ON should be asserted (high)

Note: The design should de-assert (low) MODULE_POWER_ON if VDDIN_PWR_BAD_N is asserted (low), CARRIER_POWER_ON is de-asserted (low), or MODULE_SHDN_N is asserted (low).

5.3.2 Power Button Supervisor MCU

The Jetson AGX Orin Developer Kit carrier board implements a power button supervisor. This supervisor is a low power device meant to intercept push-button (momentary) switches to control ON or Enable signals to the module PMIC and main processor. This supervisor is always powered and allows close to complete system power OFF while providing proper timing for ON and OFF signals to the system. The selected MCU to perform this function is the EFM8SB10F8G-A-QFN20 from Silicon Labs.

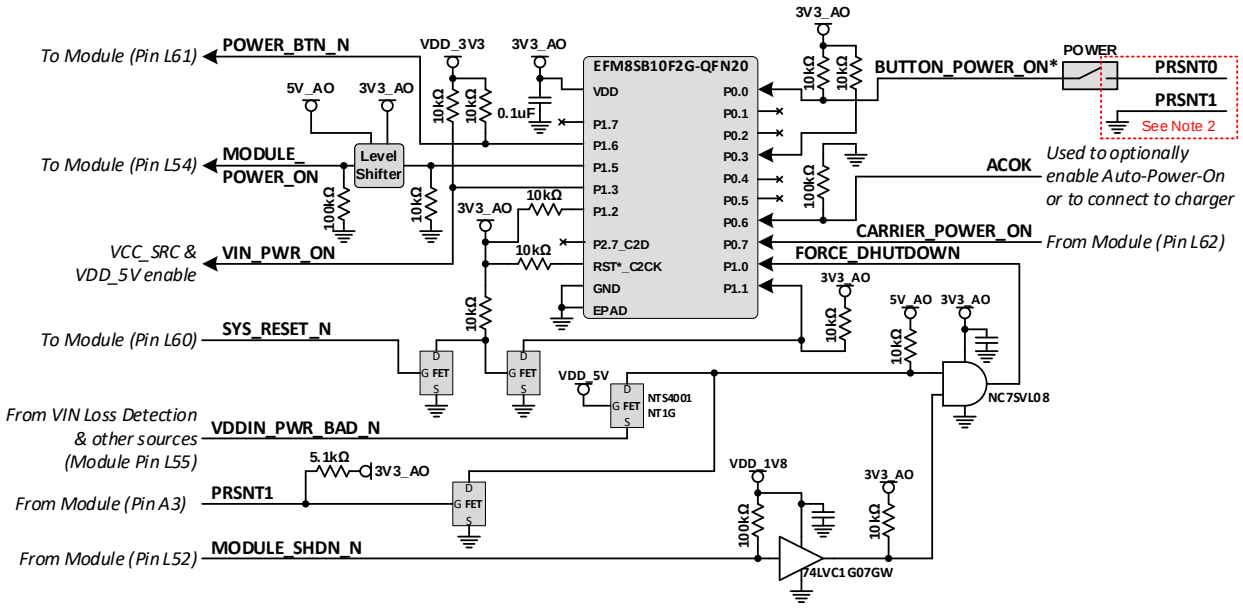
Note: Designs that intend to follow the NVIDIA carrier board design and include the EFM8SB10F8G-A-QFN20 MPU for Button Power Button control need to replicate the circuitry on the latest P3737 carrier board. NVIDIA will provide the binary and the customer should get the flashing instructions from Silicon Labs.

Table 5-2. Power Button Supervisor Control Signals

Signal Name	Associated Module Pin #	I/O Type	Trigger Level	Drive Mode	Description	MCU Pin
BUTTON_POWER_ON*		Input (debounced)	Level	OD (HiZ)	Power Button	P0.0
ACOK		Input (debounced)	Edge	OD (HiZ)	Determine when power is supplied	P0.6
CARRIER_POWER_ON	L62	Input	Level	OD (HiZ)	Closed loop on power output	P0.7
SYS_RESET_N	L60	Input	Edge	OD (HiZ)	Monitor / Power Good mask	P1.1
FORCE_SHUTDOWN_N (OVERTEMP_N)	L52	Input	Level	OD (HiZ)	Triggers shutdown sequence	P1.0
BRD_SEL		Input		OD (HiZ)	Strap pin for board selection	P1.2
VIN_PWR_ON		Output		PP	Enable power to module	P1.3
MODULE_POWER_ON	L54	Output		PP	Enable input to PMIC	P1.5
POWER_BTN_N	L61	Output		OD	Buffered output of power button signal	P1.6

Note: OD – Open-drain. PP = Push-pull.

Figure 5-7. Power-On Button Circuit



Notes:

1. Refer to the carrier board reference design for the latest connection details including different sources for ACOK.
2. Optional use of Present pins on module to ensure the power button will only initiate power-on if the module is mounted correctly. The PRSNT[1:0] pins are on opposing corners of the module connector.

5.3.2.1 Defined Behaviors

For all actions triggered by BUTTON_POWER_ON* or ACOK, there will be a de-bounce time before triggering any output signal. The minimum I/O delay for these signals is therefore the de-bounce time. De-bounce time is 20 ms. If both signals are triggered within the 20 ms de-bounce time started by the first detected signal, then the de-bounce time for the subsequent signals might extend up to 25 ms.

Note: The time values in the following timing diagrams have an accuracy of ± 10%.

5.3.2.2 Power OFF -> Power ON (Power Button Case)

Power button press use case: User presses the power button briefly, and the MCU sends the power enable signals to the module (VIN_PWR_ON) and to the PMIC on the module (MODULE_POWER_ON). The signal representing the power button to the Orin module (POWER_BTN_N), will have the same (brief) duration of the power button input to the MCU. Once the power button is pressed, the power OK input (ACOK) is ignored, as the power ON sequence is already initiated by the power button.

If power-on is successful, FORCE_SHUTDOWN_N goes high as well as CARRIER_POWER_ON.

Figure 5-8. Power-OFF to On Sequence Power Button Case

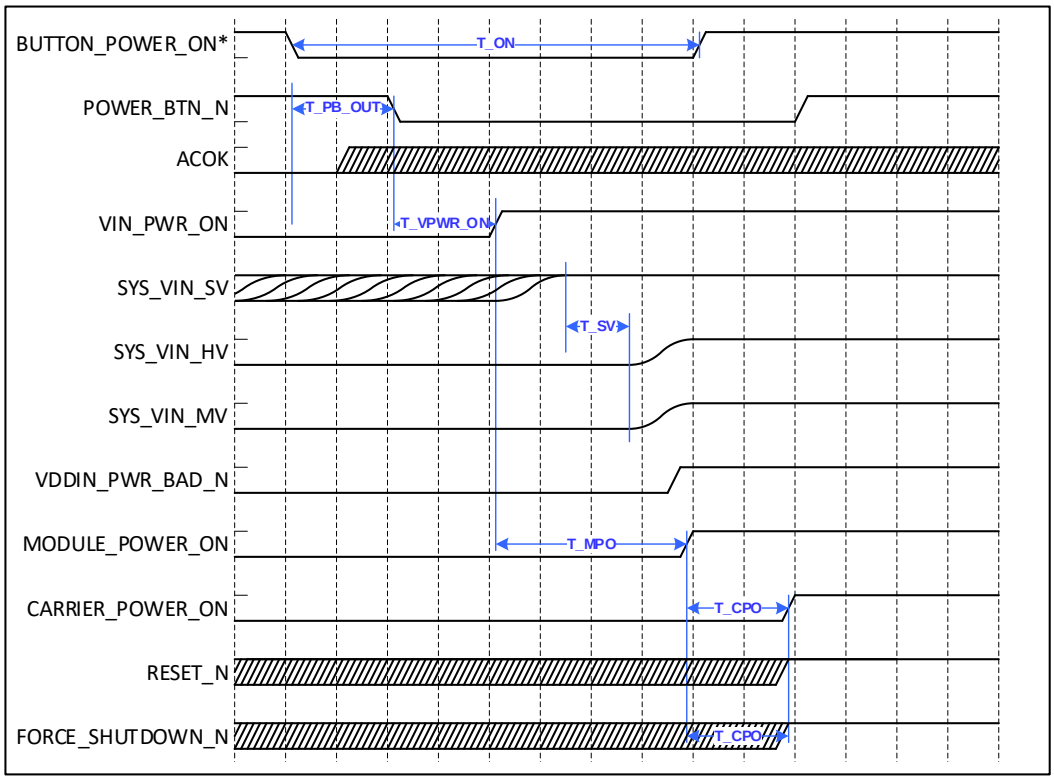


Table 5-3. Power-OFF to On Timing Power Button Case

Timing	Parameter	Typical	Units
T_ON	BUTTON_POWER_ON* minimum assertion time	20	ms
T_PB_OUT	Delay to POWER_BTN_N assertion (de-bounce only)	20	ms
T_VPWR_ON	Delay to first rail ON	0	ms
T_SV	Time delay required after SYS_VIN_SV is up and stable before SYS_VIN_HV and SYS_VIN_MV begin to power up	20 (min)	ms
T_MPO	MODULE_POWER_ON (module PMIC enable) delay from power VIN_PWR_ON rising edge	80	ms
T_CPO	Maximum allocated delay to CARRIER_POWER_ON assertion	100	ms

5.3.2.3 Power OFF -> Power ON (Auto-Power-On Case)

When the user connects the main power source, the MCU sends the power enable signals to the module (VIN_PWR_ON) and enables MODULE_POWER_ON. This is accomplished by having the ACOK signal driven high instead of pulled to GND.

The signal representing the power button to the Orin module (POWER_BTN_N) will continue following the power button (BUTTON_POWER_ON*) behavior. However, once the power ON

sequence is initiated by the connection of the main power source, and ACOK is driven high (by push-pull driver powered from 3V3_AO), the power button signals will not affect the MCU behavior until the PWR_GOOD signal verification is complete.

Figure 5-9. Power-OFF to On Sequence Auto Power-On Case

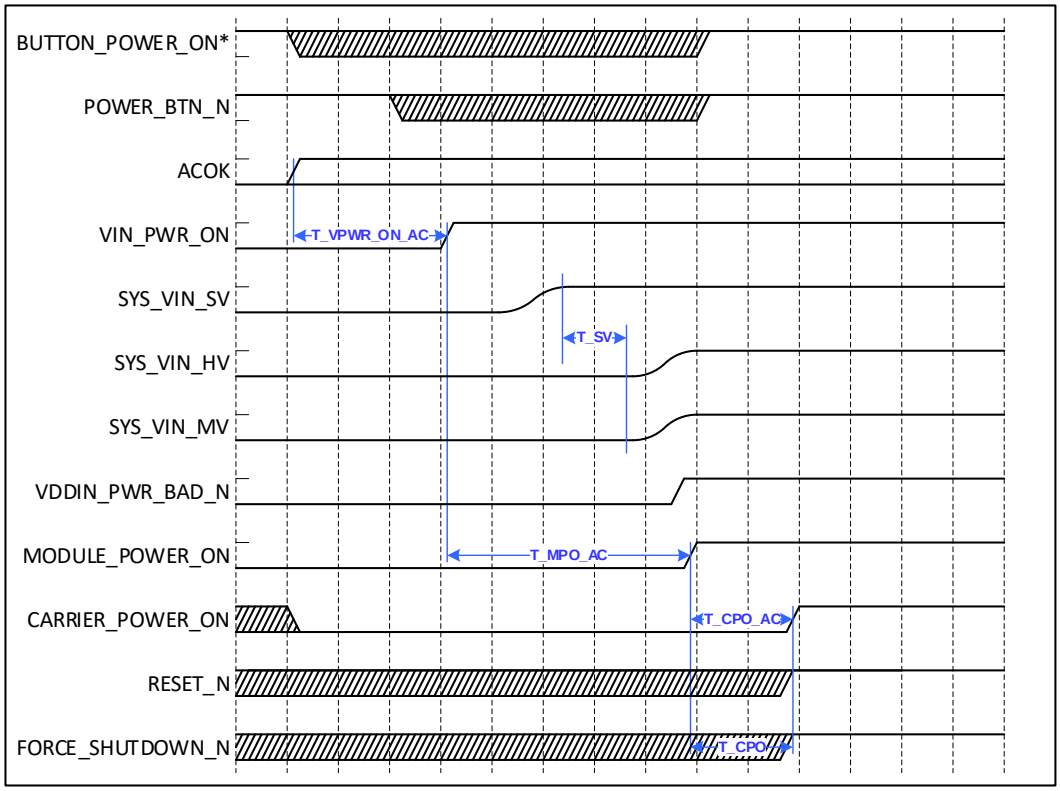


Table 5-4. Power-OFF to On Timing Auto Power-On Case

Timing	Parameter	Typical	Units
T_VPWR_ON_AC	Delay from ACOK detected high with main power source applied to first rail ON (de-bounce only)	20	ms
T_SV	Time delay required after SYS_VIN_SV is up and stable before SYS_VIN_HV and SYS_VIN_MV begin to power up	20 (min)	ms
T_MPO_AC	MODULE_POWER_ON active delay from VIN_PWR_ON rising edge	80	ms
T_CPO_AC	Maximum allocated delay to CARRIER_POWER_ON active	100	ms

5.3.2.4 Power ON -> Power OFF (Power Button Held Low > 10 Seconds)

With the system in power ON state, the user holds the power button for more than 10 seconds. The same button signal is relayed to the Orin module through the buffered signal POWER_BTN_N. The system is forced to shut down at the 10 second mark. ACOK is ignored as the sequence is initiated by the power button.

Figure 5-10. Power-On to OFF Power Button Held Low > 10 Seconds

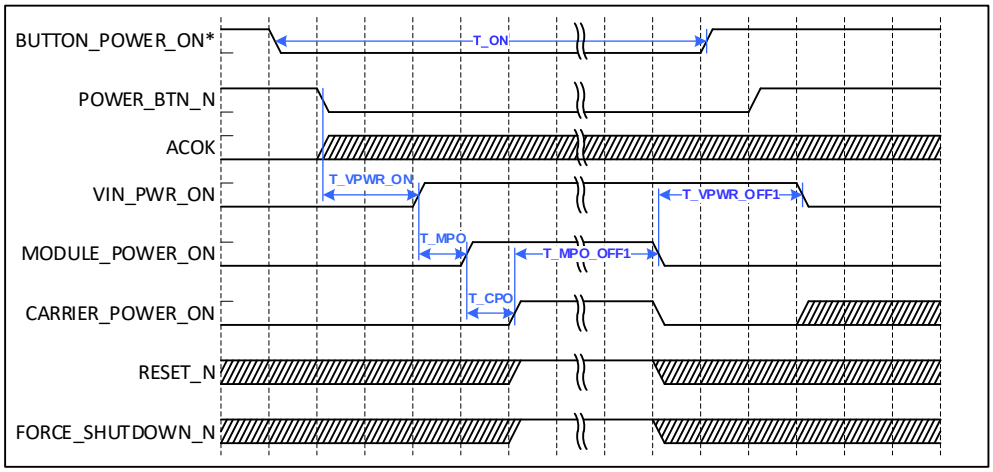


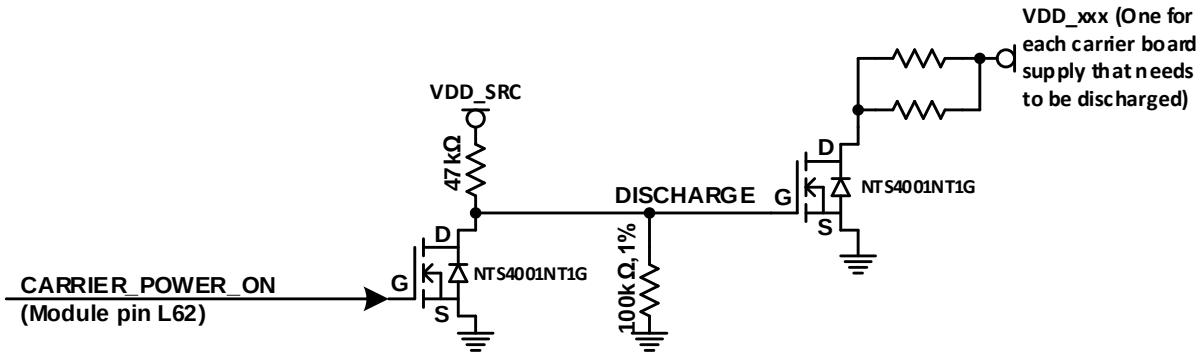
Table 5-5. Power-On to OFF Timing Power Button Held Low > 10 Seconds

Timing	Parameter	Typical	Units
T_ON	Power button active duration for forced OFF (T_PWR_ON + T_MPO_ON + T_CPO + T_MPO_OFF1)	> 10	s
T_VPWR_ON	Delay to first rail ON (de-bounce only)	20	ms
T_MPO_OFF1	Wait time to force MODULE_POWER_ON OFF	10	s
T_MPO	Enable delay from VIN_PWR_ON rising edge	80	ms
T_CPO	Maximum allocated delay to detect CARRIER_POWER_ON	100	ms
T_VPWR_OFF1	Delay to first rail OFF	10	ms

5.4 Power Discharge

To meet the power down requirements, discharge circuitry may be required. Figure 5-11 shows an example of a simplified discharge circuit. The DISCHARGE signal is generated, based on a transition of the CARRIER_POWER_ON signal or the removal of the main supply (VDD_SRC). When DISCHARGE is asserted, the various carrier board rails that need to be discharged are pulled to GND.

Figure 5-11. Power Discharge

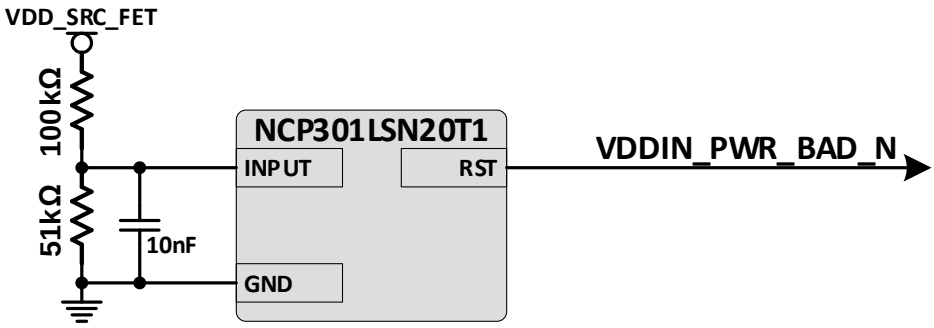


Note: The resistor values in the discharge circuit for each rail should be tuned to bring the rail down in the proper timeframe.

5.5 Power Loss Detection

The circuit in Figure 5-12 is implemented on the Orin module carrier board to detect a loss or unacceptable droop on the main power input (VCC_SRC).

Figure 5-12. VIN Loss Detection Circuit



5.6 Deep Sleep or SC7

Jetson AGX Orin supports a low power state called Deep Sleep or SC7. This can be entered under software control, and exited using various mechanisms, including wake capable pins that are listed in the pin mux. More details related to SC7 can be found at: l4t docs.

Chapter 6. General Routing Guidelines

6.1 Signal Name Conventions

The following conventions are used in describing the signals for Orin module:

- Signal names use a mnemonic to represent the function of the signal. For example, Secure Digital Interface Command signal is represented as SDCARD_CMD, with a different font to distinguish it from other text. All active low signals are identified by an underscore followed by capital N (_N) after the signal name. For example, SYS_RESET_N indicates an active low signal. Active high signals do not have the underscore-N (_N) after the signal names. For example, SDCARD_CMD indicates an active high signal. Differential signals are identified as a pair with the same names that end with _P and _N, just P and N or + and - (for positive and negative, respectively). For example, USB1_P and USB1_N indicate a differential signal pair.
- I/O Type: The signal I/O type is represented as a code to indicate the operational characteristics of the signal.

Table 6-1 lists the I/O codes used in the signal description tables.

Table 6-1. Signal Type Codes

Code	Definition
A	Analog
DIFF I/O	Bidirectional Differential Input/Output
DIFF IN	Differential Input
DIFF OUT	Differential Output
I/O	Bidirectional Input/Output
I	Input
O	Output
OD	Open Drain Output
I/OD	Bidirectional Input / Open Drain Output
P	Power

6.2 Routing Guideline Format

The routing guidelines have the following format to specify how a signal should be routed.

- Breakout traces are traces routed from a BGA or other pin array, either to a point beyond the array, or to another layer where full normal spacing guidelines can be met. Breakout trace delay limited to 12.5 mm unless otherwise specified.
- After breakout, signal should be routed according to specified impedance for differential, single-ended, or both (for example: HDMI). Trace spacing to other signals also specified.
- Follow max and min trace delays where specified. Trace delays are typically shown in mm or in terms of signal delay in pico-seconds (ps) or both.
  - For differential signals, trace spacing to other signals must be larger of specified × dielectric height or inter-pair spacing.
  - Spacing to other signals or pairs cannot be smaller than spacing between complementary signals (intra-pair).
  - Total trace delay depends on signal velocity which is different between outer (microstrip) and inner (stripline) layers of a PCB.

6.3 Signal Routing Conventions

Throughout this design guide, the following signal routing conventions are used:

SE Impedance (/ Diff Impedance) at x Dielectric Height Spacing

- Single-ended (SE) impedance of trace (along with differential impedance for diff pairs) is achieved by spacing requirement. Spacing requirements are specified as a multiple of dielectric height. Dielectric height is typically different for microstrip and stripline.

Note: Trace spacing requirement applies to SE traces or differential pairs to other SE traces or differential pairs. It does not apply to traces making up a differential pair. For this case, spacing/trace widths are chosen to meet differential impedance requirement.

6.4 Routing Guidelines

Pay close attention when routing high speed interfaces, such as HDMI, DP, USB 3.2, PCIe or CSI. Each of these interfaces has strict routing rules for the trace impedance, width, spacing, total delay, and delay or flight time matching. The following guidelines provide an overview of the routing guidelines and notations used in this design guide.

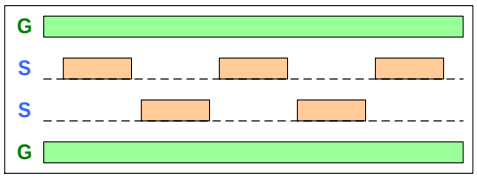
- Controlled Impedance
  Each interface has different trace impedance requirements and spacing to other traces. It is up to designer to calculate trace width and spacing required to achieve specified single-ended (SE) and differential (Diff) impedances. Unless otherwise noted, trace impedance values are ±15%.

- Max Trace Lengths and Delays
  Trace lengths and delays should include main PCB routing and any additional routing on a flex or secondary PCB segment connected to main PCB. The max length or delay should be from Orin module to the actual connector (i.e., USB, HDMI, SD Card, and so on) or device (i.e. onboard USB device, Display driver IC, camera imager IC, and so on).
- Trace Delay or Flight Time Matching
  Signal flight time is the time it takes for a signal to propagate from one end (driver) to the other end (receiver). One way to get same flight time for signal within signal group is to match trace lengths or delays within specified delay in the signal group.
  - Total trace delay = Carrier PCB trace delay only. Do not exceed maximum trace delay specified.
  - It is recommended to match trace delays based on flight time of signals. For example, outer-layer signal velocity could be 5.9 ps/mm and inner-layer 6.9 ps/mm. If one signal is routed 250 mm on the outer layer and second signal is routed 250 mm in the inner layer, the difference in flight time between two signals will be 250 ps! That is a big difference if required matching is 15 ps (trace delay matching). To fix this, inner trace needs to be 36 mm shorter or outer trace needs to be 42 mm longer.
  - In this design guide, terms such as intra-pair and inter-pair are used when describing differential pair delay. Intra-pair refers to matching traces within differential pair (for example, true to complement trace matching). Inter-pair matching refers to matching differential pairs average delays to other differential pairs average delays. For CSI CPHY, Intra-trio and inter-trio describe relative trio delays. Intra-trio refers to matching traces within the CPHY trios. Inter-trio matching refers to matching trio average delays to other trio average delays.

6.5 General PCB Routing Guidelines

For GSSG stack-up to minimize crosstalk, signal should be routed in such a way that they are not on top of each other in two routing layers (Figure 6-1).

Figure 6-1. Signal Routing Example



Do not route other signals or power traces and areas directly under or over critical high-speed interface signals.

Note: The requirements detailed in the interface signal routing requirements tables must be met for all interfaces implemented or proper operation cannot be guaranteed.

Chapter 7. USB, PCIe, and MGBE

The Orin module facilitates multiple high-speed interfaces to be brought out on the module in different configurations. The tables in this chapter show basic generic usage and descriptions of the UPHY lanes.

Table 7-1. SoC UPHY0 Data Lane Pin Descriptions (USB 3.2 and PCIe)

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
A23	UPHY_RX0_N	HS_UPHY0_L0_RX_N	UPHY block 0, Receive Lane 0	Input	UPHY Diff Pair
A22	UPHY_RX0_P	HS_UPHY0_L0_RX_P		Input	UPHY Diff Pair
C22	UPHY_RX1_N	HS_UPHY0_L1_RX_N	UPHY block 0, Receive Lane 1	Input	UPHY Diff Pair
C23	UPHY_RX1_P	HS_UPHY0_L1_RX_P		Input	UPHY Diff Pair
C35	UPHY_RX20_N	HS_UPHY0_L2_RX_N	UPHY block 0, Receive Lane 2	Input	UPHY Diff Pair
C34	UPHY_RX20_P	HS_UPHY0_L2_RX_P		Input	UPHY Diff Pair
B32	UPHY_RX21_N	HS_UPHY0_L3_RX_N	UPHY block 0, Receive Lane 3	Input	UPHY Diff Pair
B33	UPHY_RX21_P	HS_UPHY0_L3_RX_P		Input	UPHY Diff Pair
D32	UPHY_RX22_N	HS_UPHY0_L4_RX_N	UPHY block 0, Receive Lane 4	Input	UPHY Diff Pair
D33	UPHY_RX22_P	HS_UPHY0_L4_RX_P		Input	UPHY Diff Pair
A35	UPHY_RX23_N	HS_UPHY0_L5_RX_N	UPHY block 0, Receive Lane 5	Input	UPHY Diff Pair
A34	UPHY_RX23_P	HS_UPHY0_L5_RX_P		Input	UPHY Diff Pair
B13	UPHY_RX10_N	HS_UPHY0_L6_RX_N	UPHY block 0, Receive Lane 6	Input	UPHY Diff Pair
B12	UPHY_RX10_P	HS_UPHY0_L6_RX_P		Input	UPHY Diff Pair
D13	UPHY_RX11_N	HS_UPHY0_L7_RX_N	UPHY block 0, Receive Lane 7	Input	UPHY Diff Pair
D12	UPHY_RX11_P	HS_UPHY0_L7_RX_P		Input	UPHY Diff Pair
J23	UPHY_TX0_N	HS_UPHY0_L0_TX_N	UPHY block 0, Transmit Lane 0	Output	UPHY Diff Pair
J22	UPHY_TX0_P	HS_UPHY0_L0_TX_P		Output	UPHY Diff Pair
G22	UPHY_TX1_N	HS_UPHY0_L1_TX_N	UPHY block 0, Transmit Lane 1	Output	UPHY Diff Pair
G23	UPHY_TX1_P	HS_UPHY0_L1_TX_P		Output	UPHY Diff Pair
K33	UPHY_TX20_N	HS_UPHY0_L2_TX_N	UPHY block 0, Transmit Lane 2	Output	UPHY Diff Pair
K32	UPHY_TX20_P	HS_UPHY0_L2_TX_P		Output	UPHY Diff Pair
G34	UPHY_TX21_N	HS_UPHY0_L3_TX_N	UPHY block 0, Transmit Lane 3	Output	UPHY Diff Pair
G35	UPHY_TX21_P	HS_UPHY0_L3_TX_P		Output	UPHY Diff Pair
J34	UPHY_TX22_N	HS_UPHY0_L4_TX_N	UPHY block 0, Transmit Lane 4	Output	UPHY Diff Pair
J35	UPHY_TX22_P	HS_UPHY0_L4_TX_P		Output	UPHY Diff Pair
H33	UPHY_TX23_N	HS_UPHY0_L5_TX_N	UPHY block 0, Transmit Lane 5	Output	UPHY Diff Pair
H32	UPHY_TX23_P	HS_UPHY0_L5_TX_P		Output	UPHY Diff Pair
K12	UPHY_TX10_N	HS_UPHY0_L6_TX_N	UPHY block 0, Transmit Lane 6	Output	UPHY Diff Pair
K13	UPHY_TX10_P	HS_UPHY0_L6_TX_P		Output	UPHY Diff Pair

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
H13	UPHY_TX11_N	HS_UPHY0_L7_TX_N	UPHY block 0, Transmit Lane 7	Output	UPHY Diff Pair
H12	UPHY_TX11_P	HS_UPHY0_L7_TX_P		Output	UPHY Diff Pair

Notes:

1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. AC coupling capacitors are required for PCIe TX signals from both the Orin SoC and the connected PCIe device. If the connected PCIe device is on the other side of a connector, the AC capacitors should be located on the same side of the connector as the PCIe device.

Table 7-2. SoC UPHY1 Data Lane Pin Descriptions (PCIe)

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
D25	UPHY_RX12_N	HS_UPHY1_L0_RX_N	UPHY block 1, Receive Lane 0	Input	UPHY Diff Pair
D24	UPHY_RX12_P	HS_UPHY1_L0_RX_P		Input	UPHY Diff Pair
B24	UPHY_RX13_N	HS_UPHY1_L1_RX_N	UPHY block 1, Receive Lane 1	Input	UPHY Diff Pair
B25	UPHY_RX13_P	HS_UPHY1_L1_RX_P		Input	UPHY Diff Pair
C26	UPHY_RX14_N	HS_UPHY1_L2_RX_N	UPHY block 1, Receive Lane 2	Input	UPHY Diff Pair
C27	UPHY_RX14_P	HS_UPHY1_L2_RX_P		Input	UPHY Diff Pair
A27	UPHY_RX15_N	HS_UPHY1_L3_RX_N	UPHY block 1, Receive Lane 3	Input	UPHY Diff Pair
A26	UPHY_RX15_P	HS_UPHY1_L3_RX_P		Input	UPHY Diff Pair
D29	UPHY_RX16_N	HS_UPHY1_L4_RX_N	UPHY block 1, Receive Lane 4	Input	UPHY Diff Pair
D28	UPHY_RX16_P	HS_UPHY1_L4_RX_P		Input	UPHY Diff Pair
B28	UPHY_RX17_N	HS_UPHY1_L5_RX_N	UPHY block 1, Receive Lane 5	Input	UPHY Diff Pair
B29	UPHY_RX17_P	HS_UPHY1_L5_RX_P		Input	UPHY Diff Pair
C30	UPHY_RX18_N	HS_UPHY1_L6_RX_N	UPHY block 1, Receive Lane 6	Input	UPHY Diff Pair
C31	UPHY_RX18_P	HS_UPHY1_L6_RX_P		Input	UPHY Diff Pair
A31	UPHY_RX19_N	HS_UPHY1_L7_RX_N	UPHY block 1, Receive Lane 7	Input	UPHY Diff Pair
A30	UPHY_RX19_P	HS_UPHY1_L7_RX_P		Input	UPHY Diff Pair
H25	UPHY_TX12_N	HS_UPHY1_L0_TX_N	UPHY block 1, Transmit Lane 0	Output	UPHY Diff Pair
H24	UPHY_TX12_P	HS_UPHY1_L0_TX_P		Output	UPHY Diff Pair
K24	UPHY_TX13_N	HS_UPHY1_L1_TX_N	UPHY block 1, Transmit Lane 1	Output	UPHY Diff Pair
K25	UPHY_TX13_P	HS_UPHY1_L1_TX_P		Output	UPHY Diff Pair
G26	UPHY_TX14_N	HS_UPHY1_L2_TX_N	UPHY block 1, Transmit Lane 2	Output	UPHY Diff Pair
G27	UPHY_TX14_P	HS_UPHY1_L2_TX_P		Output	UPHY Diff Pair
J27	UPHY_TX15_N	HS_UPHY1_L3_TX_N	UPHY block 1, Transmit Lane 3	Output	UPHY Diff Pair
J26	UPHY_TX15_P	HS_UPHY1_L3_TX_P		Output	UPHY Diff Pair
H29	UPHY_TX16_N	HS_UPHY1_L4_TX_N	UPHY block 1, Transmit Lane 4	Output	UPHY Diff Pair
H28	UPHY_TX16_P	HS_UPHY1_L4_TX_P		Output	UPHY Diff Pair
K28	UPHY_TX17_N	HS_UPHY1_L5_TX_N	UPHY block 1, Transmit Lane 5	Output	UPHY Diff Pair
K29	UPHY_TX17_P	HS_UPHY1_L5_TX_P		Output	UPHY Diff Pair
G30	UPHY_TX18_N	HS_UPHY1_L6_TX_N	UPHY block 1, Transmit Lane 6	Output	UPHY Diff Pair
G31	UPHY_TX18_P	HS_UPHY1_L6_TX_P		Output	UPHY Diff Pair
J31	UPHY_TX19_N	HS_UPHY1_L7_TX_N	UPHY block 1, Transmit Lane 7	Output	UPHY Diff Pair
J30	UPHY_TX19_P	HS_UPHY1_L7_TX_P		Output	UPHY Diff Pair

Notes:

1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. AC coupling capacitors are required for PCIe TX signals from both the Orin SoC and the connected PCIe device. If the connected PCIe device is on the other side of a connector, the AC capacitors should be located on the same side of the connector as the PCIe device.

Table 7-3. SoC UPHY2 Data Lane Pin Descriptions (PCIe and MBGE)

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
B20	UPHY_RX2_N	HS_UPHY2_L0_RX_N	UPHY block 2, Receive Lane 0	Input	UPHY Diff Pair
B21	UPHY_RX2_P	HS_UPHY2_L0_RX_P		Input	UPHY Diff Pair
D21	UPHY_RX3_N	HS_UPHY2_L1_RX_N	UPHY block 2, Receive Lane 1	Input	UPHY Diff Pair
D20	UPHY_RX3_P	HS_UPHY2_L1_RX_P		Input	UPHY Diff Pair
A19	UPHY_RX4_N	HS_UPHY2_L2_RX_N	UPHY block 2, Receive Lane 2	Input	UPHY Diff Pair
A18	UPHY_RX4_P	HS_UPHY2_L2_RX_P		Input	UPHY Diff Pair
C18	UPHY_RX5_N	HS_UPHY2_L3_RX_N	UPHY block 2, Receive Lane 3	Input	UPHY Diff Pair
C19	UPHY_RX5_P	HS_UPHY2_L3_RX_P		Input	UPHY Diff Pair
B17	UPHY_RX6_N	HS_UPHY2_L4_RX_N	UPHY block 2, Receive Lane 4	Input	UPHY Diff Pair
B16	UPHY_RX6_P	HS_UPHY2_L4_RX_P		Input	UPHY Diff Pair
D17	UPHY_RX7_N	HS_UPHY2_L5_RX_N	UPHY block 2, Receive Lane 5	Input	UPHY Diff Pair
D16	UPHY_RX7_P	HS_UPHY2_L5_RX_P		Input	UPHY Diff Pair
A14	UPHY_RX8_N	HS_UPHY2_L6_RX_N	UPHY block 2, Receive Lane 6	Input	UPHY Diff Pair
A15	UPHY_RX8_P	HS_UPHY2_L6_RX_P		Input	UPHY Diff Pair
C14	UPHY_RX9_N	HS_UPHY2_L7_RX_N	UPHY block 2, Receive Lane 7	Input	UPHY Diff Pair
C15	UPHY_RX9_P	HS_UPHY2_L7_RX_P		Input	UPHY Diff Pair
K20	UPHY_TX2_N	HS_UPHY2_L0_TX_N	UPHY block 2, Transmit Lane 0	Output	UPHY Diff Pair
K21	UPHY_TX2_P	HS_UPHY2_L0_TX_P		Output	UPHY Diff Pair
H21	UPHY_TX3_N	HS_UPHY2_L1_TX_N	UPHY block 2, Transmit Lane 1	Output	UPHY Diff Pair
H20	UPHY_TX3_P	HS_UPHY2_L1_TX_P		Output	UPHY Diff Pair
J19	UPHY_TX4_N	HS_UPHY2_L2_TX_N	UPHY block 2, Transmit Lane 2	Output	UPHY Diff Pair
J18	UPHY_TX4_P	HS_UPHY2_L2_TX_P		Output	UPHY Diff Pair
G18	UPHY_TX5_N	HS_UPHY2_L3_TX_N	UPHY block 2, Transmit Lane 3	Output	UPHY Diff Pair
G19	UPHY_TX5_P	HS_UPHY2_L3_TX_P		Output	UPHY Diff Pair
K16	UPHY_TX6_N	HS_UPHY2_L4_TX_N	UPHY block 2, Transmit Lane 4	Output	UPHY Diff Pair
K17	UPHY_TX6_P	HS_UPHY2_L4_TX_P		Output	UPHY Diff Pair
H17	UPHY_TX7_N	HS_UPHY2_L5_TX_N	UPHY block 2, Transmit Lane 5	Output	UPHY Diff Pair
H16	UPHY_TX7_P	HS_UPHY2_L5_TX_P		Output	UPHY Diff Pair
J15	UPHY_TX8_N	HS_UPHY2_L6_TX_N	UPHY block 2, Transmit Lane 6	Output	UPHY Diff Pair
J14	UPHY_TX8_P	HS_UPHY2_L6_TX_P		Output	UPHY Diff Pair
G14	UPHY_TX9_N	HS_UPHY2_L7_TX_N	UPHY block 2, Transmit Lane 7	Output	UPHY Diff Pair
G15	UPHY_TX9_P	HS_UPHY2_L7_TX_P		Output	UPHY Diff Pair

Notes:

1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. AC coupling capacitors are required for PCIe TX signals from both the Orin SoC and the connected PCIe device. If the connected PCIe device is on the other side of a connector, the AC capacitors should be located on the same side of the connector as the PCIe device.

Table 7-4, Table 7-5, and Table 7-6 show the supported UPHY mapping for the UPHY blocks [2:0]. The mapping tables indicate which lanes of each UPHY block can be assigned for USB, PCIe, or MGBE. Only one of the supported configurations per UPHY block can be used in a design. Each UPHY block is programmed independently. It is not required to select the same configuration on all 3 UPHY blocks.

Table 7-4. UPHY0 Mapping Options (USB & PCIe)

Jetson AGX Orin Pin Names	UPHY0 Lanes	Jetson AGX Orin Functions	
		Configuration #1	Configuration #2
UPHY_RX0/TX0	Lane 0	USB 3.2 (P0)	PCIe x1 (C0), RP
UPHY_RX1/TX1	Lane 1	USB 3.2 (P1)	USB 3.2 (P1)
UPHY_RX20/TX20	Lane 2	USB 3.2 (P2)	USB 3.2 (P2)
UPHY_RX21/TX21	Lane 3	PCIe x1 (C1), RP	PCIe x1 (C1), RP
UPHY_RX22/TX22	Lane 4	PCIe x4 (C4), RP	PCIe x4 (C4), RP
UPHY_RX23/TX23	Lane 5		
UPHY_RX10/TX10	Lane 6		
UPHY_RX11/TX11	Lane 7		

Table 7-5. UPHY1 Mapping Options (PCIe)

Jetson AGX Orin Pin Names	UPHY1 Lanes	Jetson AGX Orin Functions	
		Configuration #1	Configuration #2
UPHY_RX12/TX12	Lane 0	PCIe x8 (C5), RP	PCIe x8 (C5), EP
UPHY_RX13/TX13	Lane 1		
UPHY_RX14/TX14	Lane 2		
UPHY_RX15/TX15	Lane 3		
UPHY_RX16/TX16	Lane 4		
UPHY_RX17/TX17	Lane 5		
UPHY_RX18/TX18	Lane 6		
UPHY_RX19/TX19	Lane 7		

Table 7-6. UPHY2 Mapping Options (PCIe & MGBE)

Jetson AGX Orin Pin Names	UPHY2 Lanes	Jetson AGX Orin Functions		
		Configuration #1	Configuration #2	Configuration #3
UPHY_RX2/TX2	Lane 0		PCIe x8 (C7), RP	PCIe x8 (C7), EP
UPHY_RX3/TX3	Lane 1			
UPHY_RX4/TX4	Lane 2			
UPHY_RX5/TX5	Lane 3			
UPHY_RX6/TX6	Lane 4	MGBE (C0)		
UPHY_RX7/TX7	Lane 5			
UPHY_RX8/TX8	Lane 6			
UPHY_RX9/TX9	Lane 7			

7.1 USB

Orin module supports multiple USB 2.0 and USB 3.2 ports. Each of the USB 2.0 or USB 3.2 ports can support either host or device modes. Only one USB 2.0 or USB 3.2 port can be a device at a time. Polarity inversion (P/N swapping) is supported on the USB 3.2 interfaces. There are connection examples in this section to implement either a simple USB 3.2/2.0 connection to a USB 3.2 Type A connector or to a Type C connector (Based on the NVIDIA developer kit carrier board reference design).

Notes:
1. Some non-compliant USB 3.0 devices may fail unless USB 3.2 Gen2 is disabled.
2. See Section 18.1 "USB Recovery Mode" for requirements for USB recovery mode.

USB 3.2 high-speed interface pins share UPHY lanes with PCIe. See Chapter 7 for pin descriptions.

Table 7-7. USB 2.0 Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
F13	USB0_N	HS_USB0_P0_N	USB 2.0 Port 0 Data	Bidir	USB2 Diff pair
F12	USB0_P	HS_USB0_P0_P			
C10	USB1_N	HS_USB0_P1_N	USB 2.0, Port 1 Data	Bidir	USB2 Diff pair
C11	USB1_P	HS_USB0_P1_P			
A11	USB2_N	HS_USB0_P2_N	USB 2.0, Port 2 Data	Bidir	USB2 Diff pair
A10	USB2_P	HS_USB0_P2_P			
G10	USB3_N	HS_USB0_P3_N	USB 2.0, Port 3 Data	Bidir	USB2 Diff pair
G11	USB3_P	HS_USB0_P3_P			

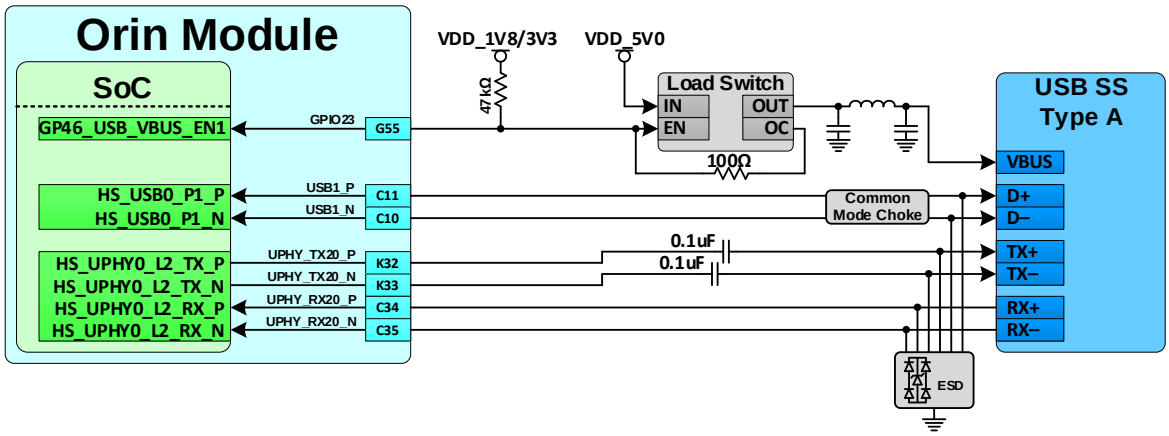
Note: In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.

Table 7-8. USB Control Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
F54	GPIO22	GP45_USB_VBUS_EN0	USB Power enable #0 or GPIO #22	Bidir	Open-Drain, 1.8V (3.3V tolerant, back-drive capable to 1.8V)
G55	GPIO23	GP46_USB_VBUS_EN1	USB Power enable #1 or GPIO #23	Bidir	

Note: In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.

Figure 7-1. Simple USB Type A Connection Example



Note:

1. A weak pull-up is required on the load switch enable and over-current connection.
2. A load switch is required between the carrier board supplies and the USB VBUS supply. The load switch should have over current protection. In Figure 7-1 this is supported by routing the over current (OC) pin of the load switch to the same pin used for the enable (GPIO23 – GP46_USB_VBUS_EN1) pin which is bidirectional and can be used to detect an over current condition.

Figure 7-2. USB Type C Connection Example

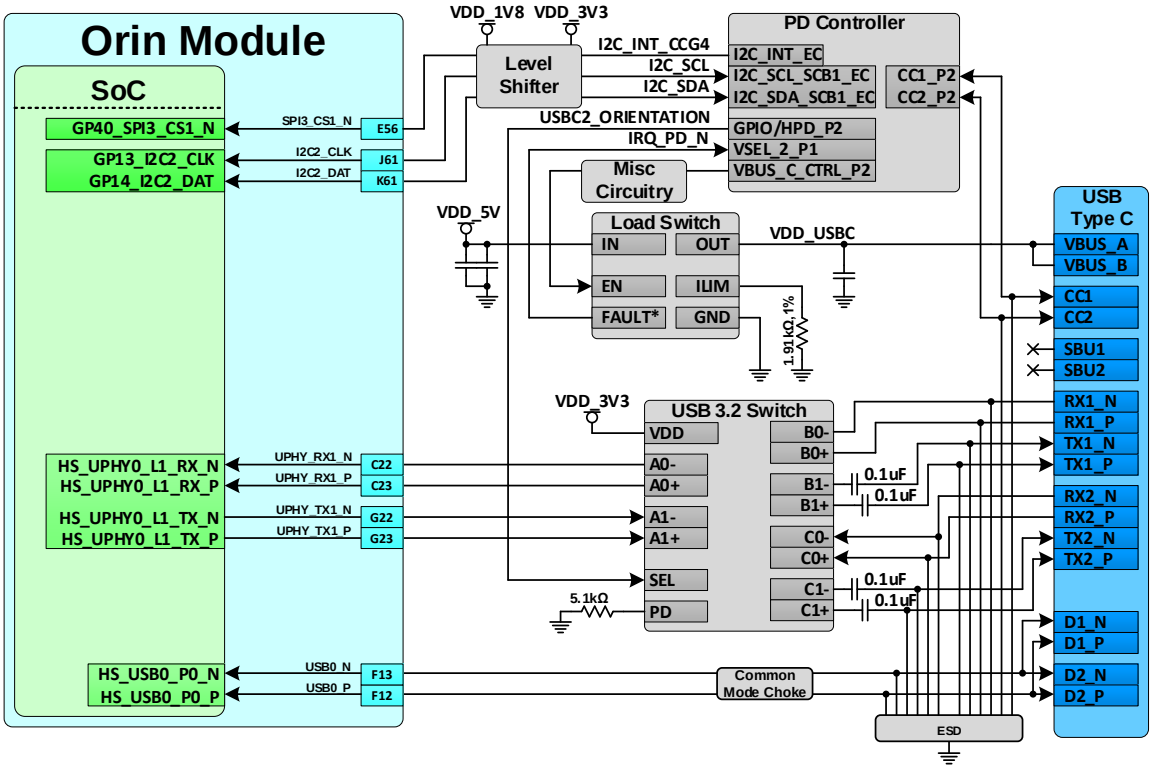


Table 7-9. USB 2.0 Signal Connections

Module Pin Name	Type	Termination	Description
USB[3:0]_N/P	DIFF I/O	90Ω common-mode chokes close to connector. ESD Protection between choke and connector on each line to GND	USB Differential Data Pair: Connect to USB connector, Mini-Card Socket, Hub, or another device on the PCB.

Table 7-10. USB 3.2 Signal Connections

Module Pin Name	Type	Termination	Description
UPHY_TX[20,1:0]_N/P (USB 3.2 Port #[2:0]	DIFF Out	Series 0.1uF AC caps. See note 1.	USB 3.2 Differential Transmit Data Pairs: Connect to USB connectors, hubs or other devices on the PCB.
UPHY_RX[20,1:0]_N/P (USB 3.2 Port #[2:0]	DIFF In	Series 0.1uF AC caps. See notes 1 and 2.	USB 3.2 Differential Receive Data Pairs: Connect to USB connectors, hubs or other devices on the PCB.

Notes:

1. Common-mode chokes (not recommended) and ESD protection if required.
2. AC caps are required on both TX and RX traces. If routing to a USB connector, AC caps should be placed on the SoC TX traces only. The AC caps for the SoC RX traces will be on the peripheral side.

7.1.1 USB 2.0 Design Guidelines

These requirements apply to the USB 2.0 controller PHY interfaces: USB[3:0]

Table 7-11. USB 2.0 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency (High Speed): Bit Rate/UI period/Freq.	480/2.083/240	Mbps/ns/MHz	
Max Loading: High Speed / Full Speed / Low Speed	10 / 150 / 600	pF	Max loading should include any passive and active components on the trace such as CMC, Switch, ESD etc.
Reference plane	GND		
Trace Impedance: Diff pair / Single Ended	90 / 50	Ω	±15%
Max Via proximity (Signal via to GND return via)	24 (3.8)	ps (mm)	
Min Pair to Pair spacing Microstrip Stripline	 4x 3x	Dielectric height	
Max Trace Delay With CMC or SW (Microstrip / Stripline) Without CMC or SW (Microstrip / Stripline)	 900/1050 (150) 1475/1720 (250)	ps (mm)	Prop delay assumption: 6.9/mm for stripline, 5.9ps/mm. for microstrip. See Note 3
Max Intra-Pair Skew between USBx_P and USBx_N	7.5	ps	

Notes:

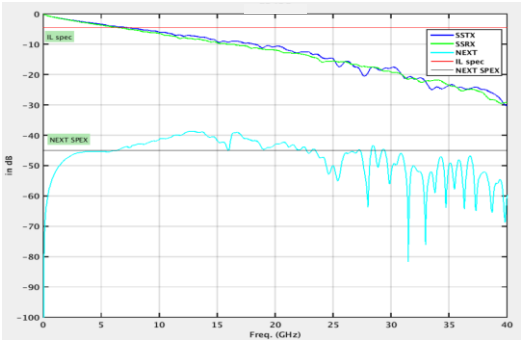
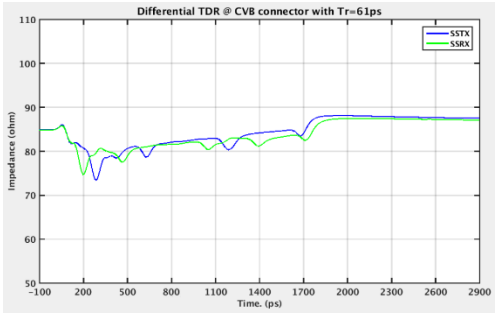
1. If portion of route is over a flex cable this length should be included in the Max Trace Length/Delay calculation and 85Ω Differential pair trace impedance is recommended.
2. Up to four signal Vias can share a single GND return Via.
3. CMC = Common-Mode-Choke. SW = Analog Switch
4. Adjustments to the USB drive strength, slew rate, termination value settings should not be necessary, but if any are made, they MUST be done as an offset to default values instead of overwriting those values.

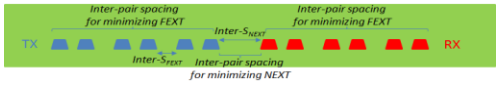
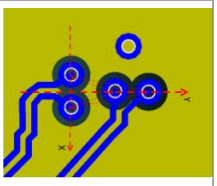
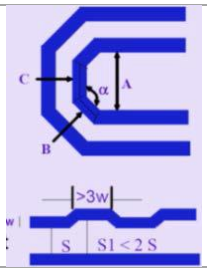
7.1.2 USB 3.2 Design Guidelines

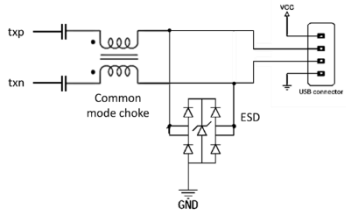
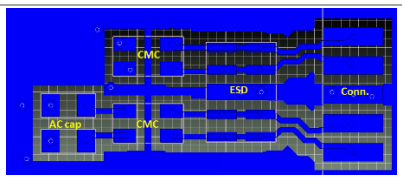
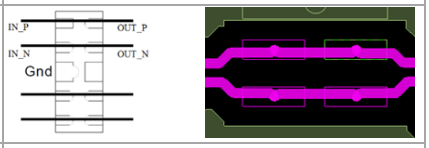
The following requirements apply to the USB 3.2 PHY interfaces. Jetson AGX Orin supports up to USB Gen2x1 (10 Gbps).

Table 7-12. USB 3.2 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI period GEN1 GEN2	 5.0 / 200 10.0 / 100	 Gbps / ps	Device mode supports GEN1 speed only.
Max Number of Loads	1	load	
Termination	90 differential	Ω	On-die termination at TX and RX

Parameter	Requirement	Units	Notes
Insertion Loss (IL) GEN1 Host (Type C) GEN1 Host (Type A) GEN1 Device (Type C) GEN1 Device (Micro AB) GEN2 Dual role mode) Resonance Dip Frequency	 ⩾ -3.8 ⩾ -7.3 ⩾ -3.8 ⩾ -2.5 [*] ⩾ -4.5 > 8	 dB @ 2.5GHz dB @ 2.5GHz dB @ 2,5GHz dB @ 2.5GHz dB @ 5GHz GHz	Only the PCB (and connector) without added-on components such as CMC, ESD, and Mux, is considered. The connector is included. For Gen2 the loss budget is the same for all connector types. For dual role mode, host and device have the same loss budget [*] the consideration of Gen1 fixture loss
Time-domain Reflectometer (TDR) Dip GEN1 GEN2	 75 75	 Ω	 @ Tr = 200ps (10%-90%) @ Tr = 61ps (10%-90%)
Near End Crosstalk (NEXT)	⩽ –45	dB	DC – 5GHz per each TX-RX NEXT
IL/NEXT Plot  		TDR Plot  	
Impedance			
Trace Impedance: Diff pair / Single Ended	85 / 43	Ω	±15%. Intrinsic differential impedance, does not account for coupling from other trace pairs
Reference plane	GND		
Trace Length (delay)/Skew			
Trace loss characteristic: GEN1 GEN2	 < 0.6 < 1	 dB/in @ 2.5 GHz dB/in @ 5G Hz	Based on the dielectric material EM370(Z). The following max length is derived based on this characteristic. The length constraint must be re-defined if the loss characteristic is changed. Note that microstrip loss could be similar to stripline due to humidity effect.
The following max length (delay) is derived based on the trace loss characteristic above. The length (delay) constraint must be re-defined if loss characteristic is changed. The trace loss profile for Gen2 support is based on the dielectric material EM370(5). See the loss plots in the sheet "USB3 LOSS BUDGET". Note that microstrip loss could be similar to stripline due to humidity effect			
Breakout Region – Max length	11	mm	Minimum trace width and spacing
Max Trace Length (delay) GEN1 Host GEN1 Device GEN2 Host or Device	 160 (1071) 107 (714) 114 (765)	mm (ps)	Stripline (6.7ps/mm) assumed. CMC use length reduction = 30mm (GEN1/2) ESD use length reduction = 10mm (GEN1), 12.5mm (GEN2).
Max Intra-Pair Skew (RX/TX_N to RX/TX_P)	0.15 (1)	mm (ps)	Do not perform length matching within breakout region. Trace length (delay) matching should be done before discontinuities. See Note 2
Differential pair uncoupled length (delay)	6.29 (41.9)	mm (ps)	

Parameter	Requirement	Units	Notes
Trace Spacing for TX/RX Non-interleaving			
TX-RX Xtalk is very critical in PCB trace routing. The ideal solution is to route TX and RX on different layers.			
If routing on the same layer, strongly recommend not interleaving TX and RX lanes			
If interleaving is required in breakout, all the inter-pair spacing should follow the rule of inter-S_{NEXT} (between TX/RX pair spacing)			
The breakout trace width is suggested to be the minimum to increase inter-pair spacing			
Do not perform serpentine routing for intra-pair skew compensation in the breakout region			
			
Min Inter-SNEXT (between TX/RX) Breakout Main-route	 4.85x 3x	Dielectric height	This is the recommended dimensions for meeting the NEXT requirement. Stripline structure in a GSSG structure is assumed (holds in broadside-coupled stripline structure)
Max length Breakout (L_{BRK}) Main-route	 11 Max trace length - L_{BRK}	mm	
Trace Spacing for TX/RX Interleaving			
Max Pair-pair spacing, Spacing to plane and SMT pad, and Spacing to unrelated high-speed signals Microstrip . Stripline	 4x / 3x	 Dielectric height	
Via			
Topology	Y-pattern is recommended. Keep symmetry		Y-pattern helps with Xtalk suppression. It can also reduce the limit of the pair-pair distance. Review needed (NEXT/FEXT check) if via placement does not use Y-pattern. 
GND via	Place GND via as symmetrically as possible to data pair vias. Up to 4 signal vias (2 diff pairs) can share a single GND return via		GND via is used to maintain return path, while its Xtalk suppression is limited
Max # of Vias PTH vias Micro Vias	 4 if all vias are PTH via Not limited		 As long as total channel loss meets IL spec
Max Via Stub Length	0.4	mm	long via stub requires review (IL and resonance dip check)
Serpentine			
Min bend angle	135	deg (a)	
Dimension Min A Spacing Min B, C Length Min Jog Width	 4x 1.5x 3x	Trace width	S1 must be taken care in order to consider Xtalk to adjacent pair. 

Parameter	Requirement	Units	Notes
Add-on Components			
Placement order	SoC – AC capacitor – Common mode choke – ESD – Device/Connector		
			
AC Cap			
Value on TX – Min/Max	100/265	nF	100nF recommended. Only required for TX pair when routed to connector.
Value on RX (connector case) – Min/Max	297/363	nF	Optional. 330nF recommended if placed.
Location (max length to adjacent discontinuity)	8	mm	Discontinuity is connector, via, or component pad
Voiding	GND/PWR void under/above cap is preferred		Voiding is required if AC cap size is 0603 or larger
ESD			
Max Junction capacitance (IO to GND) GEN1 GEN2	 0.8 0.35	pF	GEN1: e.g. SEMTECH RClamp0524p GEN2: e.g. TPD4E02B04DQA
Footprint	Pad should be on the net – not trace stub		
Location (max length to adjacent discontinuity)	8	mm	Discontinuity is connector, via, or component pad
Common-Mode Choke			
Common-mode impedance @ 100 MHz (Min/Max) GEN1 GEN2	 65/90 5/35	Ω	Gen1: TDK ACM2012D-900-2P or others having less Sdd21 Gen2: the selection priority from the min Sdd21 to the max Sdd21 NFG0QHB542HS2 -> TCM0605S_120 -> NFG0QHB372HS2 -> NFG0QHB242HS2 -> TCM0605S_350 Add CMC for fixing wifi desense problem - Wifi/BT 2.4G: NFG0QHB242HS2 - Wifi 5.0G: NFG0QHB542HS2 - if issue at 2.4G and 5G, try NFG0QHB372HS2
Max Rdc	0.3	Ω	
Differential TDR impedance	90	Ω @TR-200 ps (10%-90%)	
Min Sdd21 @ 2.5 GHz	2.22	dB	
Max Scc21 @ 2.5 GHz	19.2	dB	
Location (close to any adjacent discontinuity)	8	mm	Discontinuity: Connector, via, or other add-on components.
FPC (Additional length of Flexible Printed Circuit Board)			
The FPC routing should be included for PCB trace calculations (max length/delay, etc.)			
Characteristic Impedance	Same as PCB		
Loss characteristic	Strongly recommend to be the same as PCB or better		If worse than PCB, the PCB and FPC length (delay) must be re-estimated

Parameter	Requirement	Units	Notes
Connector			
SMT Connector GND Voiding			GND plane under signal pad should be voided. Size of void should be the same size as the pad.
Connector type			Connector used must be USB-IF certified

Notes:
1. Up to four signal Vias can share a single **GND** return Via
2. Recommend trace length/delay matching to <1ps before Vias or any discontinuity to minimize common mode conversion.
3. Place **GND** Vias as symmetrically as possible to data pair Vias.

7.1.3 Common USB Routing Guidelines

If routing to USB device or USB connector includes a flex or 2nd PCB, the total routing including all PCBs and flexes must be used for the max trace and skew calculations.

Keep critical USB related traces away from other signal traces or unrelated power traces and areas or power supply components.

Table 7-13. Recommended USB Observation Test Points for Initial Boards

Test Points Recommended	Location
One for each of the USB 2.0 data lines (USBx_N/P)	Near Orin module connector and USB device. USB connector pins can serve as test points.
One for each of the USB 3.2 output lines used (TXn_N/P)	Near USB device. USB connector pins can serve as test points
One for each of the USB 3.2 input lines (RXn_N/P)	Near Orin module connector.

7.2 PCI Express

Orin module provides 22 lanes that can be used for PCIe. Root port is supported on all PCIe interfaces. Endpoint mode is supported on Interfaces C5 and C7 only. For pin descriptions of the RX/TX lanes, see Table 7-1, Table 7-2, and Table 7-3. Lane reversal and polarity inversion (P/N swapping) is supported.

Table 7-14. PCIe Clock Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
E14	PEX_CLK0_N	SF_PCIE7_CLK_N	PCIe output Reference Clock for controller #7.	Output	PCIe Diff pair
E15	PEX_CLK0_P	SF_PCIE7_CLK_P			
F17	PEX_CLK1_N	SF_PCIE0_CLK_N	PCIe output Reference Clock for controller #0.	Output	PCIe Diff pair
F16	PEX_CLK1_P	SF_PCIE0_CLK_P			
E18	PEX_CLK2_N	SF_PCIE8_CLK_N	PCIe output Reference Clock for controller #8. Unused	Output	PCIe Diff pair
E19	PEX_CLK2_P	SF_PCIE8_CLK_P			
F21	PEX_CLK3_N	SF_PCIE10_CLK_N	PCIe output Reference Clock for controller #10. Unused	Output	PCIe Diff pair
F20	PEX_CLK3_P	SF_PCIE10_CLK_P			

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
E22	PEX_CLK4_N	SF_PCIE4_CLK_N	PCIe output Reference Clock for controller #4.	Output	PCIe Diff pair
E23	PEX_CLK4_P	SF_PCIE4_CLK_P			
F25	PEX_CLK5_N	SF_PCIE5_CLK_N	PCIe output Reference Clock for controller #5.	Output	PCIe Diff pair
F24	PEX_CLK5_P	SF_PCIE5_CLK_P			
F33	UPHY_REFCLK3_N	SF_PCIE6_CLK_N	PCIe Output Reference Clock for controller #6. Unused	Output	PCIe Diff pair
F32	UPHY_REFCLK3_P	SF_PCIE6_CLK_P			
D48	PEX_CLK6_N	SF_PCIE1_CLK_N	PCIe Output Reference Clock for controller #1.	Output	PCIe Diff pair
D49	PEX_CLK6_P	SF_PCIE1_CLK_P			
E26	UPHY_REFCLK1_N	HS_UPHY2_REFCLK1_N	UPHY block 2 Reference Clock 1. This is the REFCLK for controller #7 if used as Endpoint.	Input	PCIe Diff pair
E27	UPHY_REFCLK1_P	HS_UPHY2_REFCLK1_P			
F29	UPHY_REFCLK2_N	HS_UPHY2_REFCLK2_N	UPHY block 2 Reference Clock 2. This is the REFCLK for MGBE.	Input	PCIe Diff pair
F28	UPHY_REFCLK2_P	HS_UPHY2_REFCLK2_P			
E31	UPHY_REFCLK0_N	HS_UPHY1_REFCLK0_N	UPHY block 1 Reference Clock 0. This is the REFCLK for controller #5 if used as Endpoint.	Input	PCIe Diff pair
E30	UPHY_REFCLK0_P	HS_UPHY1_REFCLK0_P			
C38	UPHY_REFCLK4_N	HS_UPHY1_REFCLK1_N	UPHY block 1 Reference Clock 1. This is the REFCLK for controller #6 if used as Endpoint. Unused.	Input	PCIe Diff pair
C39	UPHY_REFCLK4_P	HS_UPHY1_REFCLK1_P			

Note: In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.

Table 7-15. PCIe Control Pin Descriptions

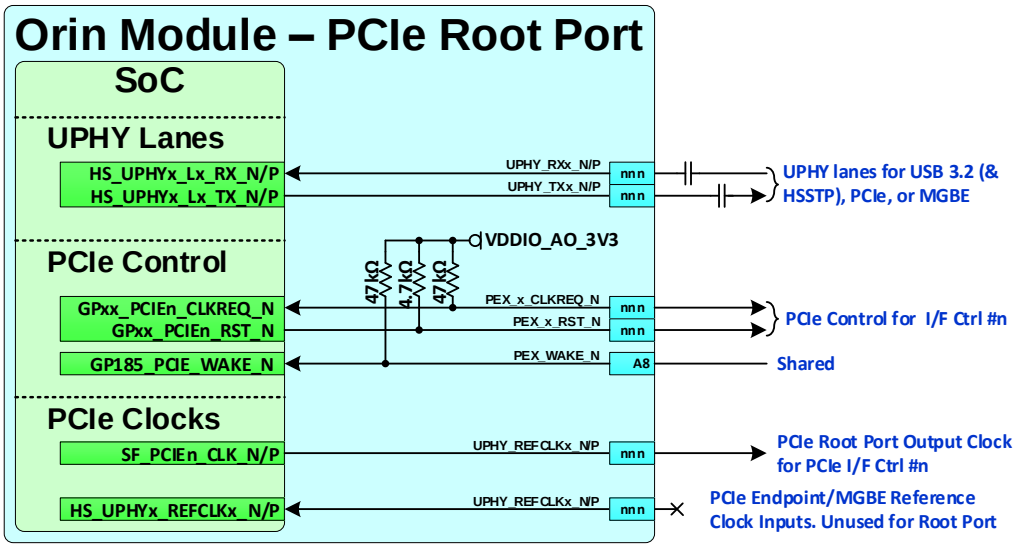
Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
E11	PEX_C0_CLKREQ_N	GP187_PCIE7_ CLKREQ_N	PCIe Clock Request for controller #7. 47KΩ pull-up to 3.3V on module.	Bidir	Open-Drain, 3.3V
D9	PEX_C1_CLKREQ_N	GP175_PCIE0_ CLKREQ_N	PCIe Clock Request for controller #0. 47KΩ pull-up to 3.3V on module.	Bidir	
J11	PEX_C2_CLKREQ_N	GP189_PCIE8_ CLKREQ_N	PCIe Clock Request for controller #8. Unused. 47KΩ pull-up to 3.3V on module.	Bidir	
J10	PEX_C3_CLKREQ_N	GP193_PCIE10_ CLKREQ_N	PCIe Clock Request for controller #10. Unused. 47KΩ pull-up to 3.3V on module.	Bidir	
G8	PEX_C4_CLKREQ_N	GP183_PCIE4_ CLKREQ_N	PCIe Clock Request for controller #4. 47KΩ pull-up to 3.3V on module.	Bidir	
C8	PEX_C5_CLKREQ_N	GP210_PCIE5_ CLKREQ_N	PCIe Clock Request for controller #5. 47KΩ pull-up to 3.3V on module.	Bidir	
L19	PEX_C6_CLKREQ_N	GP212_PCIE6_ CLKREQ_N	PCIe Clock Request for controller #6. Unused. 47KΩ pull-up to 3.3V on module.	Bidir	
B37	PEX_C7_CLKREQ_N	GP177_PCIE1_ CLKREQ_N	PCIe Clock Request for controller #1. 47KΩ pull-up to 3.3V on module.	Bidir	
A38	PEX_C8_CLKREQ_N	GP181_PCIE3_ CLKREQ_N	PCIe Clock Request for controller #3. Unused. 47KΩ pull-up to 3.3V on module.	Bidir	
D10	PEX_C0_RST_N	GP188_PCIE7_RST_N	PCIe Reset for controller #7. 4.7KΩ pull-up to 3.3V on module.	Output	Open-Drain, 3.3V
B9	PEX_C1_RST_N	GP176_PCIE0_RST_N	PCIe Reset for controller #0. 4.7KΩ pull-up to 3.3V on module.	Output	
K10	PEX_C2_RST_N	GP190_PCIE8_RST_N	PCIe Reset for controller #8. Unused. 4.7KΩ pull-up to 3.3V on module.	Output	
K9	PEX_C3_RST_N	GP194_PCIE10_ RST_N	PCIe Reset for controller #10. Unused. 4.7KΩ pull-up to 3.3V on module.	Output	
J9	PEX_C4_RST_N	GP184_PCIE4_RST_N	PCIe Reset for controller #4. 4.7KΩ pull-up to 3.3V on module.	Output	

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
H10	PEX_C5_RST_N	GP211_PCIE5_RST_N	PCIe Reset for controller #5. 4.7KΩ pull-up to 3.3V on module.	Output	
L18	PEX_C6_RST_N	GP213_PCIE6_RST_N	PCIe Reset for controller #6. Unused. 4.7KΩ pull-up to 3.3V on module.	Output	
B36	PEX_C7_RST_N	GP178_PCIE1_RST_N	PCIe Reset for controller #1. 4.7KΩ pull-up to 3.3V on module.	Output	
A39	PEX_C8_RST_N	GP182_PCIE3_RST_N	PCIe Reset for controller #3. Unused. 4.7KΩ pull-up to 3.3V on module.	Output	
A8	PEX_WAKE_N	GP185_PCIE_ WAKE_N	PCIe Wake. Wake signal shared by all PCIe interfaces. 47KΩ pull-up to 3.3V on module.	Input	

Notes:

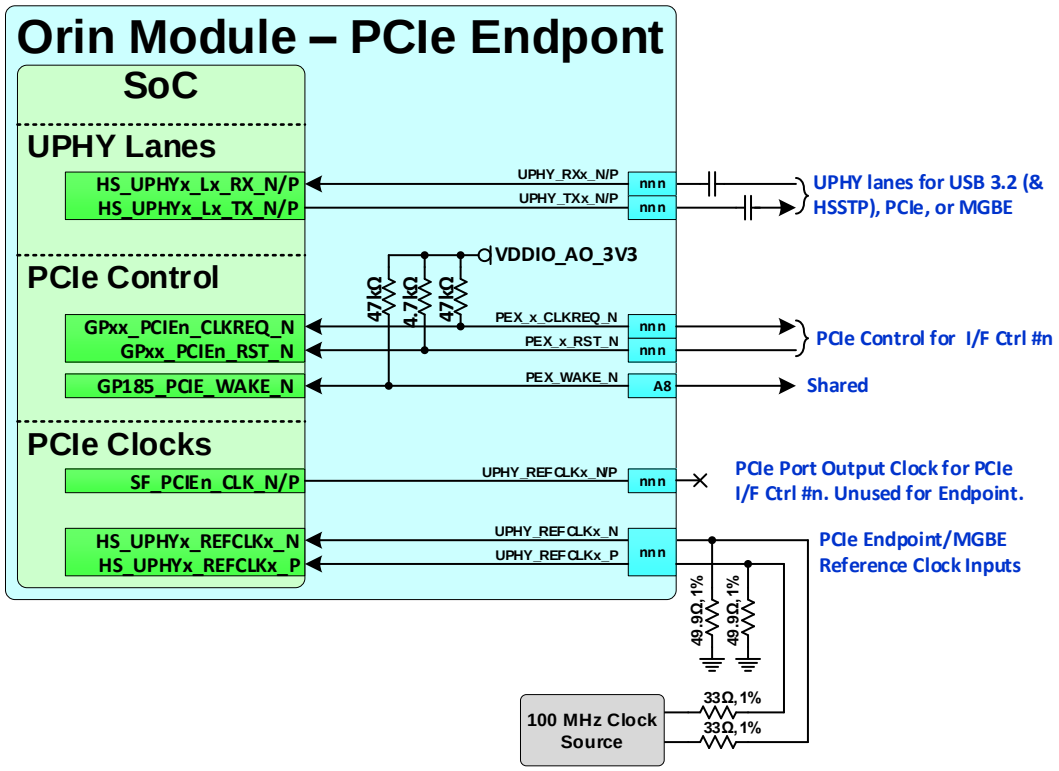
1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. The direction shown in this table for PEX_Cx_RST_N and PCIE_WAKE_N signals is true when used for those PCIe functions. Otherwise, if used as GPIOs, the direction is bidirectional.

Figure 7-3. PCIe Signal Connections (Root Port)



Note: See notes under Figure 7-3.

Figure 7-4. PCIe Signal Connections (Endpoint)



Notes:

- AC Capacitors required on SoC RX lines (Device TX lines) on carrier board if connected directly to device. They are not placed on the carrier board if connected to a PCIe or M.2 connector. In those cases, the AC caps are on the adapter board plugged into those connectors.
- See design guidelines for correct AC capacitor values.
- The PCIe RX/TX signals comply to the PCIe SIG requirements and are HCSL compatible.
- The PCIe REFCLK inputs and PCIEx_CLK clock outputs comply to the PCIe CEM specification "REFCLK DC Specifications and AC Timing Requirements." The clocks are HCSL compatible.

Table 7-16. PCIe Signal Connections Module I/Fs Configured as Root Ports

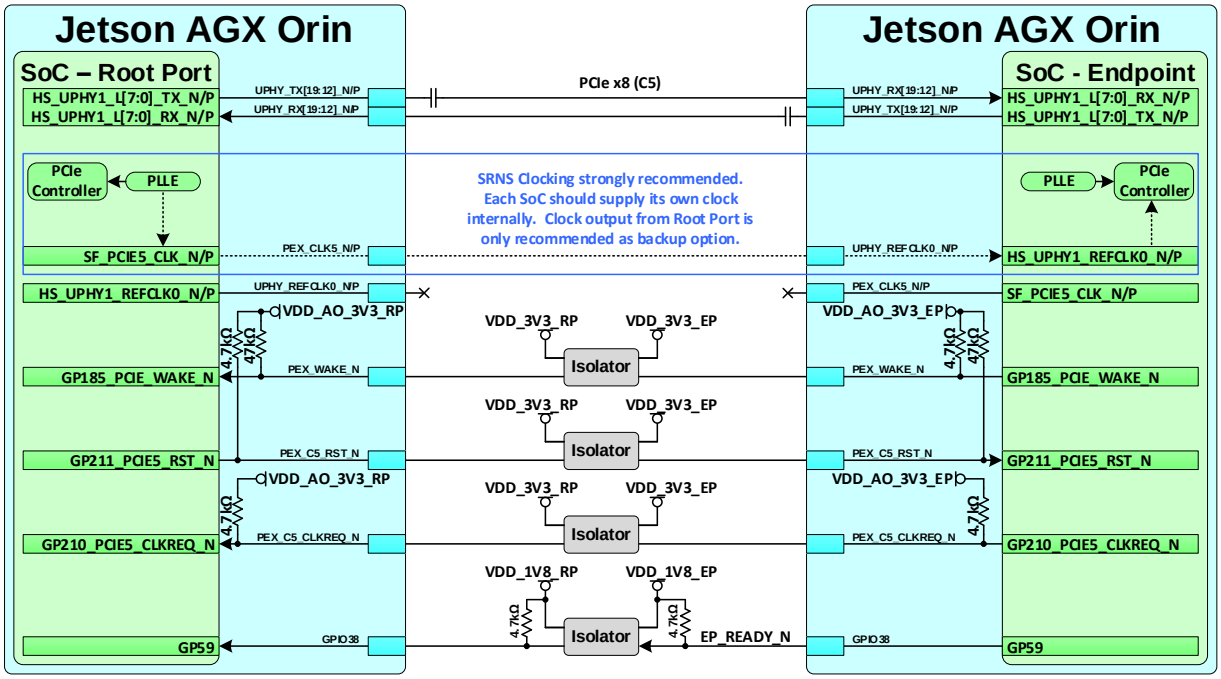
Module Pin Name	Type	Termination	Description
PCIe Interface C0 (x1) – As Root Port (only Root Port Supported)			
UPHY_TX0_P/N (SoC UPHY0 Lane 0)	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit Data Pair: Connect to TX+/– pins of PCIe connector or RX_+/– pins of PCIe device through AC caps.
UPHY_RX0_P/N (SoC UPHY0 Lane 0)	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	Differential Receive Data Pair: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.
PEX_CLK1_N/P	DIFF OUT	Series capacitors are typically not required. Check Endpoint device requirement.	Differential Reference Clock Output: Connect to REFCLK_+/– pins of PCIe device/connector.
PEX_C1_CLKREQ_N	I/O	47 kΩ pullup on module to VDDIO_AO_3V3.	PEX Clock Request for UPHY_REFCLKx: Connect to CLKREQ pin on device/connector(s)
PEX_C1_RST_N	O	4.7 kΩ pullup on module to VDDIO_AO_3V3	PEX Reset: Connect to PERST pin on device/connector.
PCIe Interface C1 (x1) – As Root Port (only Root Port Supported)			
UPHY_TX21_P/N (SoC UPHY0 Lane 1)	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit Data Pair: Connect to TX+/– pins of PCIe connector or RX_+/– pins of PCIe device through AC caps.
UPHY_RX21_P/N (SoC UPHY0 Lane 1)	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	Differential Receive Data Pair: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.
PEX_CLK6_N/P	DIFF OUT		Differential Reference Clock Output: Connect to REFCLK_+/– pins of PCIe device/connector.
PEX_C7_CLKREQ_N	I/O	47 kΩ pullup on module to VDDIO_AO_3V3.	PEX Clock Request for UPHY_REFCLKx: Connect to CLKREQ pin on device/connector(s)
PEX_C7_RST_N	O	4.7 kΩ pullup on module to VDDIO_AO_3V3	PEX Reset: Connect to PERST pin on device/connector.
PCIe Interface C4 (Up to x4) – As Root Port (only Root Port Supported)			
UPHY_TX[11:10,23:22]_P/N (SoC UPHY0 Lanes [7:4]	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit Data Pair: Connect to TX+/– pins of PCIe connector or RX_+/– pins of PCIe device through AC caps.
UPHY_RX[11:10,23:22]_P/N (SoC UPHY0 Lanes [7:4]	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	Differential Receive Data Pair: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.
PEX_CLK4_N/P	DIFF OUT		Differential Reference Clock Output: Connect to REFCLK_+/– pins of PCIe device/connector.
PEX_C4_CLKREQ_N	I/O	47 kΩ pullup on module to VDDIO_AO_3V3.	PEX Clock Request for UPHY_REFCLKx: Connect to CLKREQ pin on device/connector(s)
PEX_C4_RST_N	O	4.7 kΩ pullup on module to VDDIO_AO_3V3	PEX Reset: Connect to PERST pin on device/connector.
PCIe Interface C5 (Up to x8) – As Root Port			
UPHY_TX[19:12]_P/N (SoC UPHY1 Lanes [7:0]	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit Data Pair: Connect to TX+/– pins of PCIe connector or RX_+/– pins of PCIe device through AC caps.
UPHY_RX[19:12]_P/N (SoC UPHY1 Lanes [7:0]	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	Differential Receive Data Pair: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.
PEX_CLK5_N/P	DIFF OUT		Differential Reference Clock Output: Connect to REFCLK_+/– pins of PCIe device/connector.
PEX_C5_CLKREQ_N	I/O	47 kΩ pullup on module to VDDIO_AO_3V3.	PEX Clock Request for UPHY_REFCLKx: Connect to CLKREQ pin on device/connector(s)

Module Pin Name	Type	Termination	Description
PEX_C5_RST_N	O	4.7 kΩ pullup on module to VDDIO_AO_3V3	PEX Reset: Connect to PERST pin on device/connector.
PCIe Interface C7 (Up to x8) – As Root Port			
UPHY_TX[9:2]_P/N (SoC UPHY2 Lanes [7:0]	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit Data Pair: Connect to TX+/– pins of PCIe connector or RX_+/– pins of PCIe device through AC caps.
UPHY_RX[9:2]_P/N (SoC UPHY2 Lanes [7:0]	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	Differential Receive Data Pair: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.
PEX_CLK0_N/P	DIFF OUT		Differential Reference Clock Output: Connect to REFCLK_+/– pins of PCIe device/connector.
PEX_C0_CLKREQ_N	I/O	47 kΩ pullup on module to VDDIO_AO_3V3.	PEX Clock Request for UPHY_REFCLKx: Connect to CLKREQ pin on device/connector(s)
PEX_C0_RST_N	O	4.7 KΩ pullup on module to VDDIO_AO_3V3	PEX Reset: Connect to PERST pin on device/connector.
Common			
PEX_WAKE_N	I	47 KΩ pullup to VDDIO_AO_3V3 on Module.	PEX Wake: Connect to WAKE pins on devices or connectors

Table 7-17. PCIe Signal Connections Module I/F Configured as Endpoint

Module Pin Name	Type	Termination	Description
PCIe Interface C5 (Up to x8) – As Endpoint			
UPHY_TX[19:12]_P/N (SoC UPHY1 Lanes [7:0]	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit Data Pairs: Connect to TX+/– pins of PCIe connector or RX_+/– pin of PCIe device through AC caps.
UPHY_RX[19:12]_P/N (SoC UPHY1 Lanes [7:0]	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	Differential Receive Data Pairs: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.
UPHY_REFCLK0_N/P	DIFF IN	33 Ω series resistors near clock source. 49.9Ω resistors to GND on each line near Endpoint device. AC caps if required by clock source device.	Differential Reference Clock Input: Connect to 100 MHz clock source or REFCLK_+/– pins of PCIe connector.
PEX_C5_CLKREQ_N	I/O	47 kΩ pullup on module to VDDIO_AO_3V3.	PEX Clock Request: Connect to CLKREQ pin on device/connector.
PEX_C5_RST_N	I	4.7 kΩ pullup on module to VDDIO_AO_3V3	PEX Reset: Connect to PERST pin on device/connector.
PCIe Interface C7 (Up to x8) – As Endpoint			
UPHY_TX[9:2]_P/N (SoC UPHY2 Lanes [7:0]	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit Data Pairs: Connect to TX+/– pins of PCIe connector or RX_+/– pin of PCIe device through AC caps.
UPHY_RX[9:2]_P/N (SoC UPHY2 Lanes [7:0]	DIFF IN	Series Capacitor (see Design Guideline for value) if device on main PCB.	Differential Receive Data Pairs: Connect to RX_+/– pins of PCIe connector or TX_+/– pin of PCIe device through AC caps.
UPHY_REFCLK1_N/P	DIFF IN	33 Ω series resistors near clock source. 49.9Ω resistors to GND on each line near Endpoint device. AC caps if required by clock source device.	Differential Reference Clock Input: Connect to 100 MHz clock source or REFCLK_+/– pins of PCIe connector.
PEX_C0_CLKREQ_N	I/O	47 kΩ pullup on module to VDDIO_AO_3V3.	PEX Clock Request: Connect to CLKREQ pin on device/connector.
PEX_C0_RST_N	I	4.7 kΩ pullup on module to VDDIO_AO_3V3	PEX Reset: Connect to PERST pin on device/connector.
Common			
PEX_WAKE_N	I	47 kΩ pullup to VDDIO_AO_3V3 on Module.	PEX Wake: Unused for interfaces configured as Endpoint

Figure 7-5. PCIe Jetson AGX Orin RP to Jetson AGX Orin EP connection Example



Note: Figure 7-5 is an example showing PCI controller #5 (C5) for both Root Port and Endpoint. Other configurations are possible using C5, or C7 for either the Root Port or Endpoint.

Table 7-18. PCIe Signal Connections AGX Orin RP to AGX Orin EP

Module Pin Name	Type	Termination	Description
UPHY_TX[19:12]_P/N UPHY_RX[19:12]_P/N (SoC UPHY1 Lanes [7:0]	DIFF OUT	Series Capacitor (see Design Guideline for value)	Differential Transmit/Receive Data Pairs: Connect AGX Orin Root Port TX pins to AGX Orin Endpoint RX pins through AC caps. Connect AGX Orin Endpoint TX pins to AGX Orin Root Port RX pins through AC caps.
PEX_CLK5_P/N	DIFF OUT		PCIe Reference Clocks (ctrl C5). Connect PEX_CLK5 from Root Port AGX Orin to UPHY_REFCLK0_P/N of Endpoint AGX Orin. Back-up if SRNS option is used.
UPHY_REFCLK0_P/N	DIFF IN		
PEX_C5_CLKREQ_N (ctrl C5) Root Port Endpoint	 I O	Isolation between RP and EP (see Figure 7-5).	PCIe Clock Request for PEX_CLK5_P/N (ctrl C5). Connect to CLKREQ_N pin on each Orin device connected (RP to EP).
PEX_C5_RST_N (ctrl C5) Root Port Endpoint	 O I	Isolation between RP and EP (see Figure 7-5).	PCIe Reset: Connect to RST_N pin on each Orin device connected (RP to EP).
PEX_WAKE_N Root Port Endpoint	 I O	Isolation between RP and EP (see Figure 7-5).	PCIe Wake: Connect to WAKE pin on each ORIN device connected (RP to EP).

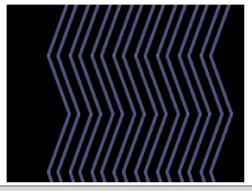
Module Pin Name	Type	Termination	Description
Endpoint Ready (EP_READY_N) GPIO38 (ctrl C5) Root Port Endpoint Pins are recommendations. Other GPIOs can be used. See Description.	 I O	Isolation between RP and EP with 4.7 kΩ pull-ups to 1.8V rail associated with GPIO each side (see Figure 7-5).	EP Ready: Connect from Orin Root Port (RP) to equivalent pin on the Orin Endpoint (EP). Pin should have pin type DD and power-on-reset value = tristated. Signal is driven low by the EP to indicate to the RP that is it ready to link. Root Port (RP). The RP will have configured the GPIO as an interrupt and will have a pullup. When the signal goes low, the RP will attempt to link to the EP.

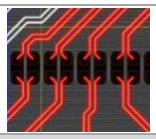
Note: The table includes mention of only C5. C7 can also be an Endpoint. If used, the CLKREQ and RST pins associated with that controller would be used. The Endpoint Ready signal can be the one shown for C5 if that controller is not used in this configuration. Alternately, another GPIO (or GPIOs) can be chosen. Any GPIO used should be DD type and tristate at power-on.

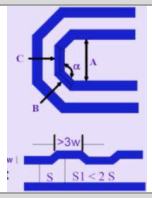
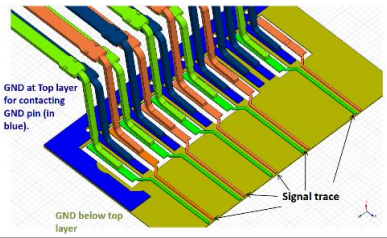
7.2.1 PCIe Design Guidelines up to Gen4

Table 7-19 details the PCIe design guidelines up to Gen4.

Table 7-19. PCIe Interface Signal Routing Requirements up to Gen4

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI Period	16.0 / 62.5	Gbps / ps	
Topology	Point-point		Unidirectional, differential. Driven by 100MHz common reference clock
Termination	43	Ω	To **GND** Single Ended for P and N
Impedance			
Trace Impedance differential / Single Ended	 85 / 50	 Ω	±15%
Reference plane	GND		
Fiber-weave effect (Only required for GEN4)	• Use spread-glass (denser weave) instead of regular-glass (sparse weave) to minimize intra-pair skew • Use zig-zag route instead of straight to minimize skew, this is a mandatory for PCIe gen4 design		Example of zig-zag routing 
Spacing			
Trace Spacing (Stripline) Pair – Pair To plane and capacitor pad To unrelated high-speed signals	 4x 4x 4x	Dielectric height	TX and RX should not be routed on the same layer. If this is required in a design, they should not be interleaved, and the spacing between the closest RX and TX lanes must be 9x Dielectric height spacing.

Parameter	Requirement	Units	Notes
Length/Skew			
Breakout region (Max delay)	41.9	ps	Minimum width and spacing. 4x or wider dielectric height spacing is preferred
Gen 4.0 max trace: Direct to device: Insertion loss / length (delay) Routing to 2nd Orin Module Insertion loss / length (delay) Routing to M.2 (NVMe) connector/card: Insertion loss / length (delay)	 -20.51 / 345 (2208) -14.74 / 248 (1587) -11.01 / 185 (1185)	dB / mm (ps)	Direct to device Insertion loss budget is for PCB routing, connectors, and end device (See Note 1). EM-370(Z) PCB material is assumed in the length/delay calculations: Gen 4.0: -1.51 dB/in @ 8Ghz Gen 3.0: -0.86 dB/in @ 4GHz Length to delay calculations assumes 6.4 ps/mm (average of stripline & microstrip). The 2nd Orin Module loss assumption is: Gen 4.0: -8 dB @ 8GHz Gen 3.0: -6.5 dB @4GHz The M.2 connector/card loss assumption is: Gen 4.0: -9.5 dB @ 8GHz Gen 3.0: -8.2 dB @4GHz
Gen 3.0 max trace: Direct to device: Insertion loss / length (delay) Routing to 2nd Orin Module Insertion loss / length (delay) Routing to M.2 (NVMe) connector/module: Insertion loss / length (delay)	 -15.8 / 467 (2987) -10.5 / 310 (1985) -7.6 / 224 (1437)	dB / mm (ps)	
Max PCB via delay from the Device/Connector	41.9	ps	Max distance from Device ball or Connector pin to first PCB via.
PCB within pair (intra-pair) skew	0.15 (1)	mm (ps)	Do trace length (delay) matching before hitting discontinuities.
Within pair (intra-pair) matching between subsequent discontinuities	0.15 (1)	mm (ps)	
Differential pair uncoupled delay	41.9	ps	
Via			
Via placement	Place **GND** vias as symmetrically as possible to data pair vias. **GND** via distance should be placed less than 1x the diff pair via pitch		
Max # of Vias	4		Use micro via or back drilled via - no via stub allowed.
Max Via stub length	N/A		Not Allowed
AC Cap			
Value Min/Max	0.22	uF	20%, 0402 X5R or better. Only required for TX pair when routed to connector. Place close to TX side.
Voiding	Voiding the plane directly under the pad ~0.1mm larger than the pad size is required.		
Serpentine (See USB 3.2 Guidelines)			

Parameter	Requirement	Units	Notes
Serpentine			
Min bend angle	135	deg (a)	S1 must be taken care in order to consider Xtalk to adjacent pair 
Dimension Min A Spacing Min B, C Length Min Jog Width	 4x 1.5x 3x	Trace width	
Miscellaneous			
GND fill rule	Remove unwanted GND fill that is either floating or act like antenna		
Connector			
Voiding	Void all layers of golden finger area under the pad ~0.15mm larger than the pad size is recommended.		
Keep critical PCIe traces such as PEX_TX/RX, etc. away from other signal traces or unrelated power traces/areas or power supply components			

Note: The trace length/delay for "Direct to device" does not account for the losses of the end device loss and any connectors involved. The loss should first be adjusted by subtracting the end device / connector losses. The length/delay may also need to be adjusted if the PCB material loss is different than the EM-370(Z) PCB material assumed.

Figure 7-6. Insertion Loss S-Parameter Plot (SDD21)

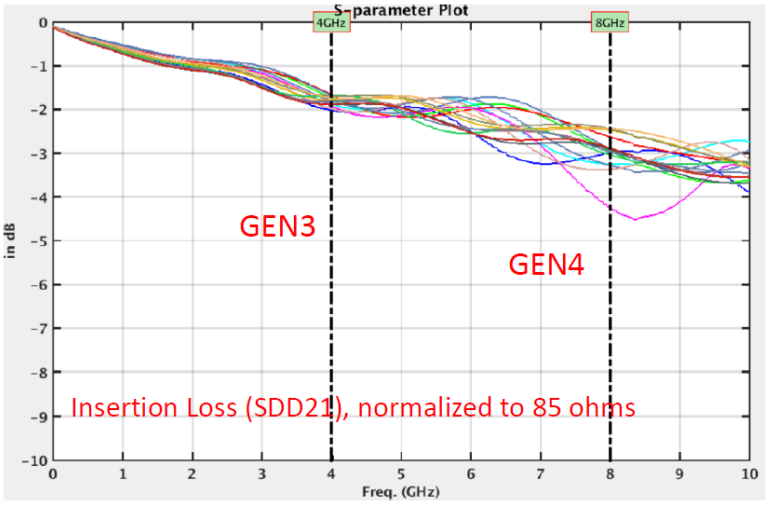


Figure 7-7. Insertion Loss S-Parameter Plot (SDD11)

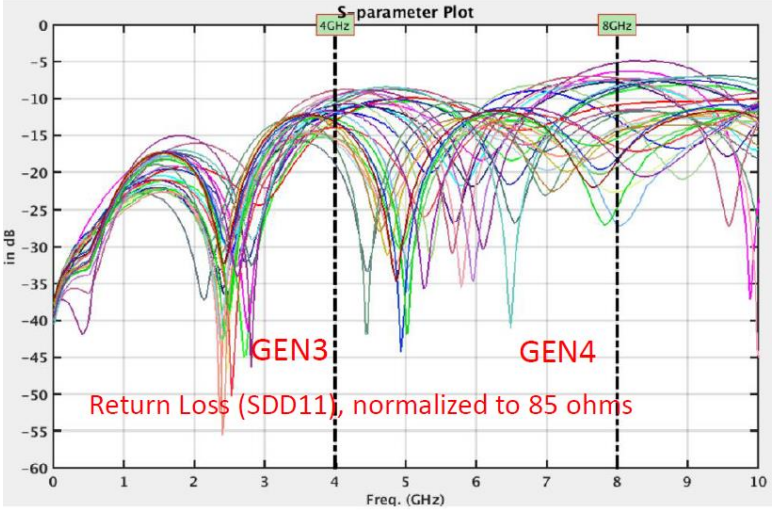


Table 7-20. Recommended PCIe Observation Test Points for Initial Boards

Test Points Recommended	Location
One for each of the PCIe **TX_+/**– output lines used.	Near PCIe device. Connector pins may serve as test points if accessible.
One for each of the PCIe **RX_+/**– input lines used.	Near Orin module connector.

7.3 MGBE

The Orin module supports one of the four Multi-Gigabit Ethernet (MGBE) interfaces on the Orin SoC: MGBE Controller #0. Communication between the Orin MGBE controller and external devices (for example, Ethernet PHYs and switches) can be achieved by XFI or SFI differential connections, supporting 5 Gbps and 10 Gbps line rates on XFI or SFI lanes.

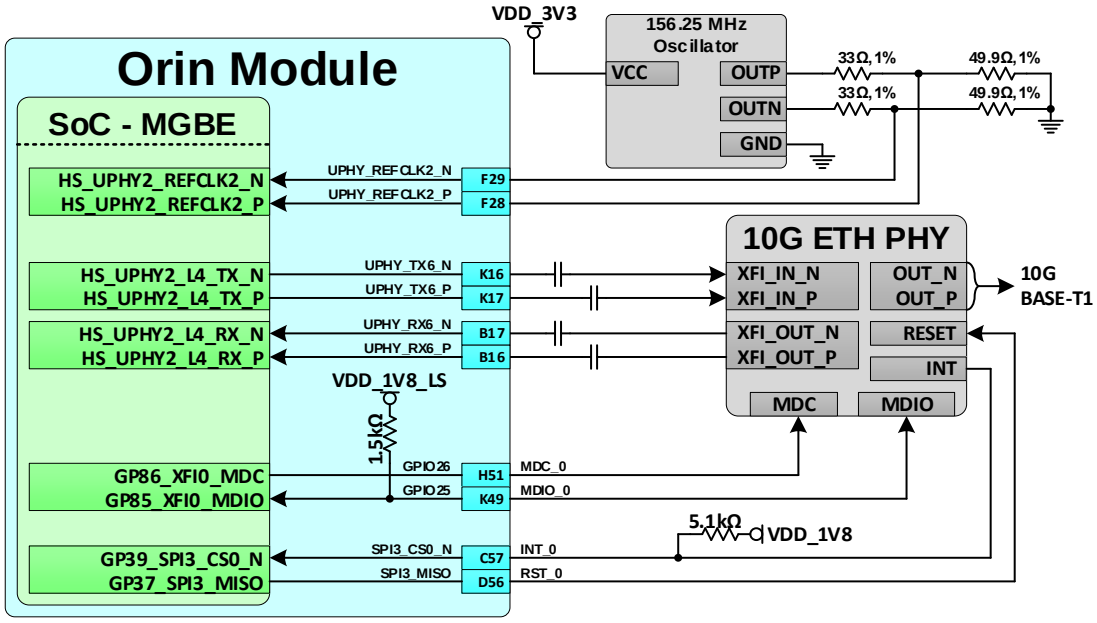
Table 7-21. MGBE MDIO Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
H51	GPIO26	GP86_XFI0_MDC	MGBE C0 Management Clock	Bidir	CMOS – 1.8V
K49	GPIO25	GP85_XFI0_MDIO	MGBE C0 Management Data	Bidir	CMOS – 1.8V

Note: In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.

An example of MGBE connection between Orin module MGBE and 10G Ethernet PHY can be seen in the Figure 7-8.

Figure 7-8. MGBE Connection Example – 10G Ethernet PHY



Note: See Table 7-25 for correct AC capacitor values.

Table 7-22. MGBE Signal Connections

Pin (Function) Name	Type	Termination	Description
MGBE0			
UPHY_RX6_N/P	DIFF IN	100nF	MGBE0 RX differential signal: Connect to TX_P/N of external PHY/Switch device through AC caps
UPHY_TX6_N/P	DIFF OUT	100nF	MGBE0 TX differential signal: Connect to RX_P/N of external PHY/Switch device through AC caps
SPI3_MISO (RST_0)	O		Connect to Reset input of external PHY or Switch
SPI3_CS0_N (INT_0)	I		Connect to Interrupt output of external PHY or Switch
Common			
UPHY_REFCLK2_P/N	DIFF IN		MGBE Reference Clock: Connect to external 156.25 MHz oscillator specified in Table 7-24. For connection details, please refer to Figure 7-8.

7.3.1 MDIO Interface

Management Data Input/Output (MDIO) interface is a two signal serial bus defined for the Ethernet family of IEEE 802.3 standards. The Orin module MGBE interface has an MDIO interface as shown in Table 7-23. This interface can be connected to external PHY or switch, allowing Orin to access the control and status registers of these devices.

Table 7-23. MGBE MDIO Signal Connections

Signal Name	Type	Termination	Description
MGBE0			
GPIO25 (MDIO_0)	I/O	1.5kΩ to 1.8V on module	MGBE0 MD IO: Connect to MDIO pin of external PHY or switch.
GPIO26 (MDC_0)	O		MGBE0 MD Clock: Connect to MDC pin of external PHY or switch
Note: The maximum operating frequency of the MD Clock is 2.5 MHz, as per IEEE 802.3 Standard			

Table 7-24. MGBE Interface Reference Clock Oscillator Requirements

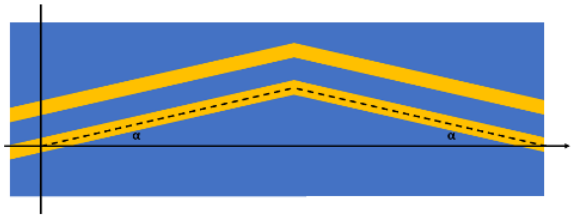
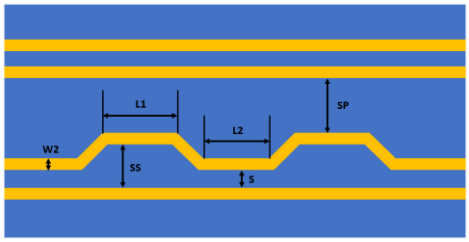
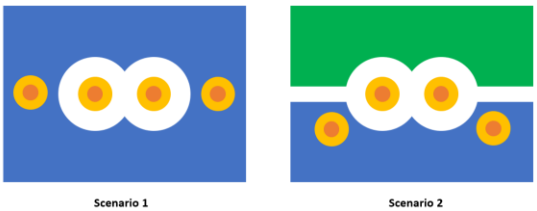
Parameter	Min	Typ	Max	Unit	Condition
Output Frequency		156.250000		MHz	
Output Driver Type		HCSL			
Frequency Stability	-100	–	+100	ppm	Inclusive of initial tolerance, aging, operating temperature, rated power supply voltage and load variations.
L_100k		-120		dBc/Hz	Phase noise at 100 kHz (typical value given for reference)
Duty Cycle	45	–	55	%	
JITrefclk	–	0.5	1.2	ps	Integrate from 12 kHz to 20 MHz
AMPrefclk	0.3	-	1.8	Vppd	Differential Voltage Swing
VCMrefclk	0.25		0.55	Vcm	Common mode
TRrefclk	0.2	1	2	ns	Rise/Fall time, 10 to 90%
Zdiff_reclk	78	85	105	Ohm	Differential trace impedance
Zcm_refclk	22.5	25	27.5	Ohm	CM trace impedance

7.3.2 MGBE Design Guidelines

The guidelines provided below apply mainly to XFI (or SFI) interface operating at 10.3125 Gbps data rate. Although overly conservative, these guidelines also apply to 5,15625 Gbps data rate as well.

Table 7-25. MGBE Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI Period	10.3125 / 97	Gbps / ps	
Configuration / Device Organization	1	Load	
Topology	Point-point		Unidirectional, differential
Termination	50	Ω	To GND Single Ended for P and N
Transmission line	Stripline		See Note 1
Impedance Control			
Target Impedance (differential)	100	Ω	See Note 2
Main Trace Impedance (differential)	95 to 105 90 to 100	Ω Ω	Valid for 100Ω target impedance Valid for 95Ω target impedance
Connector area impedance (differential)	85 to 110	Ω	
Reference plane	GND		Ground reference should be solid. Referencing to power plane or partial ground plane (some portion is power plane, and some portion is ground plane) is not allowed under any circumstance.
Spacing			
Min. Trace Spacing between: TX and RX pairs TX/RX. pairs and unrelated High-Speed structures TX/RX pairs and other Low-Seed structures TX/RX pairs and edge of reference plane TX/RX pairs and power structures (plane, via or traces)	(Stripline/MS) 7x / 10x 9x / 12x 7x / 10x 4x / 8x 7x / 10x	Dielectric height	When defining the spacing for stripline, the shortest distance to the adjacent reference plane should be considered. Route TX and RX on separate layers whenever possible. See note 3 and note 4.
Length (delay) and Skew			
Trace Loss Budget	4.6	dB @5.5GHz	See Note 5
Max trace length (delay)	106 (730)	mm (ps)	See Note 5 and Note 6.
PCB within pair (intra-pair) skew	≤ 0.13 (1)	mm (ps)	Do trace length (delay) matching before hitting discontinuities. See Note 7.
Differential pair uncoupled **total** delay	41.9	ps	
Fiber-weave compensation	To minimize intra-pair skew, the following is recommended: • Use spread-glass (denser weave) PCB material instead of regular-glass (sparse weave). • Zig-zag should be used instead of straight routing. The angle (α) of the zig-zag routing should be higher than or equal to 10 degrees.		

Parameter	Requirement	Units	Notes
	Example of zig-zag routing: 		
Serpentine geometry	The serpentine geometry is shown on the right-side figure and must satisfy the following: $L1 \geq 3 \times W2$ $L2 \geq 1.5 \times L1$ $SS \leq 2 \times S$ SP should comply to the main routing spacing rule.		
	Example of serpentine geometry: 		
Via			
GND vias placement	Place **GND** vias as symmetrically as possible to data pair vias. There should be at least one GND via associated with one signal via of a differential pair. **GND** via should be placed less than 1x the diff pair via pitch.		
Max # of layer transitions for TX/RX	4		Do not count connection between micro-vias or micro-vias and core vias in HDI designs as layer transition.
Max via stub length	0.3	mm	• Longer via stubs would require review. • Backdrill recommended for PTH stack-up, unless the impedance target can be satisfied without it.
Via void	• For PTH (Plated Through Hole) design: void all layers in the stack-up. • For HDI design: void all signaling layers, including area under (or above) the transition layer via pad.		
Via reference plane	Vias should only reference to one type of plane, e.g. GND plane (or power plane which is not recommended) as shown in Scenario 1 below. Referencing vias to partial plane or multiple planes (see Scenario 2) is not recommended. 		
Stitching vias (via fence)	Recommended for better isolation in case main route of TX/RX pair is close to other signals and signal to signal spacing is marginal.		
AC Capacitor			

Parameter	Requirement	Units	Notes
Value	100	nF	AC coupling capacitors should be placed close to receiving device.
Max. distance from discontinuity	6.5	mm	
Voiding	Voiding the plane directly under the pad ~0.1mm larger than the pad size is recommended.		Example of void under the capacitor pad: 
Miscellaneous			
Conductor bends	The bending corner should be either rounded or bevel, as shown in Scenario 2 below. Routing with 90 degrees (Scenario 1) is not accepted. 		
Routing signals over void, pad and antipads	Not allowed under any circumstance		

Notes:

1. Stripline routing is strongly recommended for better crosstalk performance. The two reference planes of the stripline should be solid ground layer. Microstrip routing is to be used for breakout region (usually connecting AC cap). If microstrip is needed for the entire channel, tighter trace-to-trace spacing spec should be applied.
2. For the main route, if 100Ω is not achievable due to stack-up limitation, the target impedance can be relaxed to 95Ω.
3. If routing on different layers are not applicable due to other routing constraints, routing TX and RX pairs on the same layer is acceptable if the separation between these pairs are at least 7x and 10x for stripline and microstrip respectively.
4. If components at both ends of the channel are placed on the same layer (e.g. all on top layer or all on bottom layer), RX routing layer should be the layer closer to component placement layer while TX routing layer can be further from the component placement layer (e.g. components all on top layer, RX on L3, TX on L5).
5. The max. trace length/delay and insertion loss already account for the effects of Orin module board-to-board connector. In case extra connectors or devices are added in the path between Orin module MGBE signals and Ethernet MAC/PHY device, then the max. trace length (and delay) and insertion loss should be re-evaluated.
6. Trace length/delay is defined considering a PCB material loss of 1.1dB/inch at 5.5GHz. For PCB materials with higher loss, the max. trace length/delay must be shortened. For PCB materials with lower loss, max. trace length/delay may be relaxed.
7. Include only PCB trace lengths/delays for Differential P/N matching. The SoC package delays for differential signal pairs are adequately matched. Do length/delay matching before via transitions to different layers or any discontinuity to minimize common mode conversion.

Chapter 8. Gigabit Ethernet

The Orin module provides an RGMII interface to support 1 Gigabit Ethernet functionality. As shown in Figure 8-1 and Figure 8-2, the Ethernet PHY, magnetics and RJ45 connector are not included on Orin module and must be implemented externally to the Orin module.

Table 8-1. Orin Module Gigabit Ethernet Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
K7	RGMII_TX_CTL	GP152_RGMII0_TX_CTL	Ethernet Transmit Control	Output	CMOS – 1.8V
B5	RGMII_TXC	GP147_RGMII0_TXC	Ethernet Transmit Clock	Output	CMOS – 1.8V
J6	RGMII_TD0	GP148_RGMII0_TD0	Ethernet Transmit data bit 0	Output	CMOS – 1.8V
G5	RGMII_TD1	GP149_RGMII0_TD1	Ethernet Transmit data bit 1	Output	CMOS – 1.8V
J7	RGMII_TD2	GP150_RGMII0_TD2	Ethernet Transmit data bit 2	Output	CMOS – 1.8V
G6	RGMII_TD3	GP151_RGMII0_TD3	Ethernet Transmit data bit 3	Output	CMOS – 1.8V
D5	RGMII_RX_CTL	GP157_RGMII0_RX_CTL	Ethernet Receive Control	Input	CMOS – 1.8V
C5	RGMII_RXC	GP158_RGMII0_RXC	Ethernet Receive Clock	Input	CMOS – 1.8V
C4	RGMII_RD0	GP153_RGMII0_RD0	Ethernet Receive data bit 0	Input	CMOS – 1.8V
K6	RGMII_RD1	GP154_RGMII0_RD1	Ethernet Receive data bit 1	Input	CMOS – 1.8V
H6	RGMII_RD2	GP155_RGMII0_RD2	Ethernet Receive data bit 2	Input	CMOS – 1.8V
E5	RGMII_RD3	GP156_RGMII0_RD3	Ethernet Receive data bit 3	Input	CMOS – 1.8V
E6	RGMII_SMA_MDC	GP160_RGMII0_SMA_MDC	Ethernet Management Clock	Output	CMOS – 1.8V
E7	RGMII_SMA_MDIO	GP159_RGMII0_SMA_MDIO	Ethernet Management Data	Bidir	CMOS – 1.8V
H5	ENET_RST_N	GP112	Ethernet Reset	Bidir	CMOS – 1.8V
J5	ENET_INT	GP111	Ethernet Interrupt	Bidir	CMOS – 1.8V

Note: In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.

Figure 8-1. Ethernet Connections

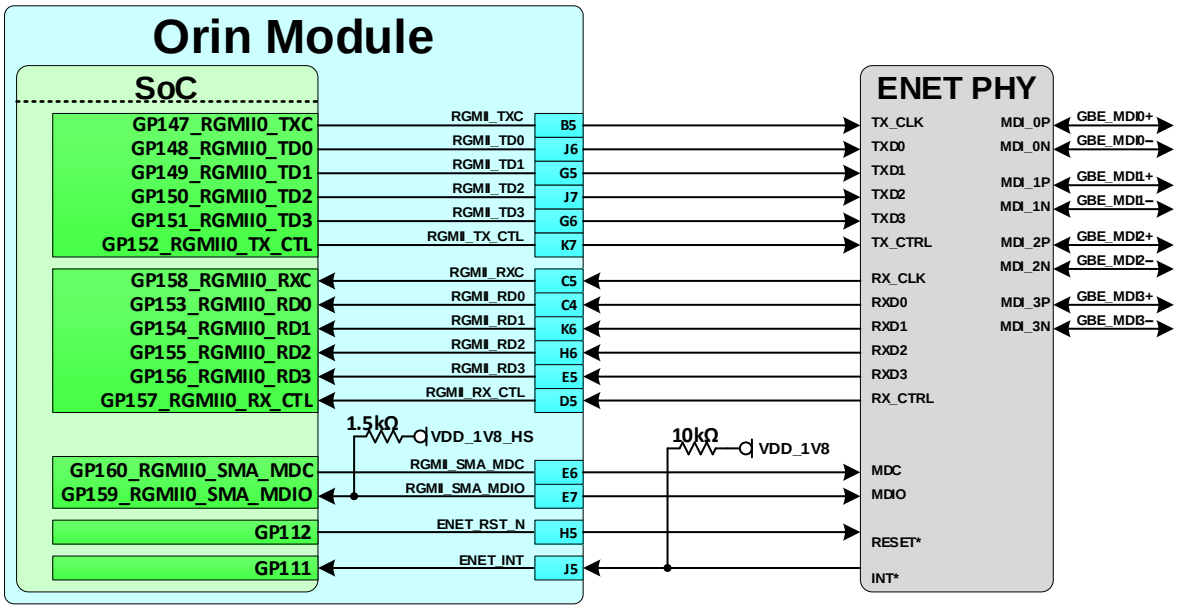
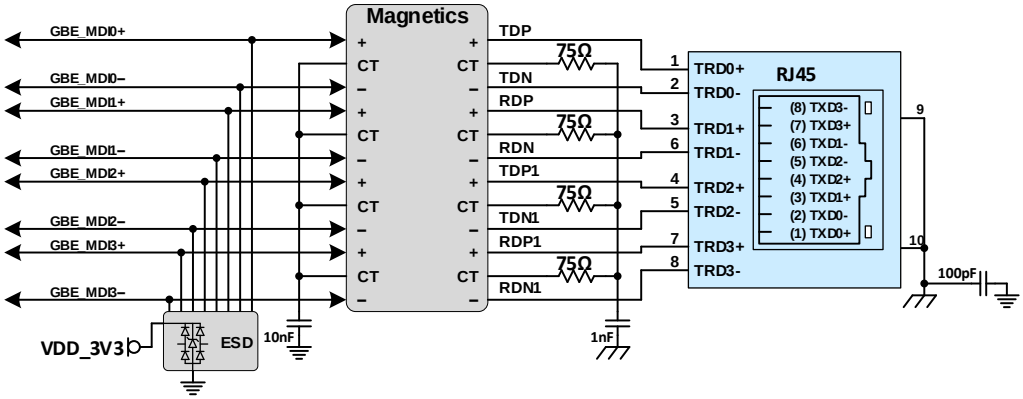


Figure 8-2. Gigabit Ethernet Magnetics and RJ45 Connections



Note: The connections in Figure 8-2 match those used on the carrier board and are shown for reference only.

Table 8-2. Ethernet Signal Connections

Module Pin Name	Type	Termination	Description
RGMII_TXC	O		RGMII Transmit Clock: Connect to TXCLK pin on GbE Transceiver.
RGMII_TD[3:0]	O		RGMII Transmit Data: Connect to TXD[3:0] pins on GbE Transceiver.
RGMII_TX_CTL	O		RGMII Transmit Control: Connect to TXEN pin on GbE Transceiver.
RGMII_RXC	I		RGMII Receive Clock: Connect to RXCLK pin on GbE Transceiver.
RGMII_RD[3:0]	I		RGMII Receive Data: Connect to RXD[3:0] pins on GbE Transceiver.

Module Pin Name	Type	Termination	Description
RGMII_RX_CTL	I		RGMII Receive Control: Connect to RXDV pin on GbE Transceiver.
RGMII_MDC	O		MDC: Connect to MDC pin on GbE Transceiver.
RGMII_MDIO	I/O	1.5kΩ pull-up to VDD_1V8_HS on the module	MDIO: Connect to MDIO pin on GbE Transceiver.
ENET_RST_N	O		Ethernet Reset: Connect to Reset input on Ethernet PHY.
ENET_INT	I	10kΩ pull-up to VDD_1V8	Ethernet Interrupt: Connect to Interrupt output on Ethernet PHY.

Note: Refer to the relevant device manufacturer guidelines for correct connections from the SoC input and output clock, data, control to device.

8.1 RGMII Design Guidelines

Table 8-3 shows the signal routing requirements for RGMII interface.

Table 8-3. RGMII Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency	125	MHz	
Topology	Point to point		Unidirectional, source terminated, source synchronous
Reference plane	GND		
Trace Impedance	50	Ω	±15%
Max breakout distance	12 (75)	mm (ps)	
Via proximity (Signal via to GND return via)	< 3.8 (24)	mm (ps)	See note 1
Trace spacing: Microstrip / Stripline	4x / 3x	dielectric height	
Max Trace Length (Delay)	265 (1670)	mm (ps)	Assumes a propagation delay of 6.3 ps/mm.
Max Trace Delay Skew Between Clock and Data MAC/PHY supports RGMII-ID (Internal Delay) MAC/PHY does not support RGMII-ID	 8 (50) See note 2	mm (ps)	
Isolation of TX and RX CLK signals	One of the following options for **TX_CLK** and **RX_CLK** signals: **GND** shielding from each other and any other signal, or >5x spacing from each other and any other signal, or Routed on separate layers and >5x spacing from other signals.		
Isolation of TX and RX groups	One of the following options for **TX** signal and **RX** signal groups: **GND** shielding from each other, or >5x spacing from each other, or Routed on separate layers from each other		

Parameter	Requirement	Units	Notes
Noise Coupling Avoidance	Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components		

Notes:

1. Up to 4 signal vias can share a single GND return via
2. NVIDIA Orin SoC does not support RGMII-ID (Internal Delay) feature, meaning that Orin RGMII TX CLK and DATA are edge aligned, while Orin RGMII RX CLK and DATA must be center aligned. Therefore, a CLK-to-DATA skew of greater than 1.5ns and less than 2.0ns must be ensured on Orin RGMII RX signals, either via MAC/PHY RGMII-ID (if supported) or via PCB trace delay. The requirements and recommendations of MAC/PHY RGMII Receiver shall be followed for the CLK-to-DATA skew of Orin RGMII TX signals.

Table 8-4. Recommended Ethernet Test Points for Initial Boards

Test Points Recommended	Location
One for each of the RGMII lines.	TX near the device and RX near the Orin module connector

Chapter 9. Display

Orin module supports a standard DP 1.4 or HDMI™ v2.1 interface. They share the same set of interface pins, so either DisplayPort or HDMI can be supported natively. Multi-head support through MST is included. Refer to the *NVIDIA Jetson AGX Orin Module Data Sheet* for the maximum resolutions supported.

Note: MST is only supported on DisplayPort.

Table 9-1. Orin Module HDMI, eDP, and DP Pin Description

Module Pin #	SoC Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
D52	F49	HDMI_DP2_TX0_N	HS_DISP0_HDMI_D2_DP0_N	DisplayPort 2 Lane 0 or HDMI Lane 2. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
D51	F50	HDMI_DP2_TX0_P	HS_DISP0_HDMI_D2_DP0_P			
B52	H51	HDMI_DP2_TX1_N	HS_DISP0_HDMI_D1_DP1_N	DisplayPort 2 Lane 1 or HDMI Lane 1. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
B51	H50	HDMI_DP2_TX1_P	HS_DISP0_HDMI_D1_DP1_P			
A50	F51	HDMI_DP2_TX2_N	HS_DISP0_HDMI_D0_DP2_N	DisplayPort 2 Lane 2 or HDMI Lane 0. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
A51	F52	HDMI_DP2_TX2_P	HS_DISP0_HDMI_D0_DP2_P			
C50	G49	HDMI_DP2_TX3_N	HS_DISP0_HDMI_CK_DP3_N	DisplayPort 2 Lane 3 or HDMI Clk Lane. AC-Coupled on carrier board.	Output	HDMI/DP Diff pair
C51	G50	HDMI_DP2_TX3_P	HS_DISP0_HDMI_CK_DP3_P			
K50		DP2_HPD	GP74_HPD0_N	Display Port/HDMI 2 Hot Plug Detect	Bidir	CMOS – 1.8V
J50		HDMI_CEC	GP05_HDMI_CEC	HDMI CEC	Bidir	Open Drain, 1.8V (3.3V tolerant
G53		DP2_AUX_CH_P	SF_DPAUX01_P	Display Port 2 Aux+ or HDMI DDC SCL. AC-Coupled on Carrier Board for DP AUX (eDP/DP) or pulled high for DDC/I2C.	Bidir	Open-Drain, 1.8V (3.3V tolerant)
G54		DP2_AUX_CH_N	SF_DPAUX01_N	Display Port 2 Aux– or HDMI DDC SDA. AC-Coupled on Carrier Board for DP AUX (eDP/DP) or pulled high for DDC/I2C.	Bidir	Open-Drain, 1.8V (3.3V tolerant)

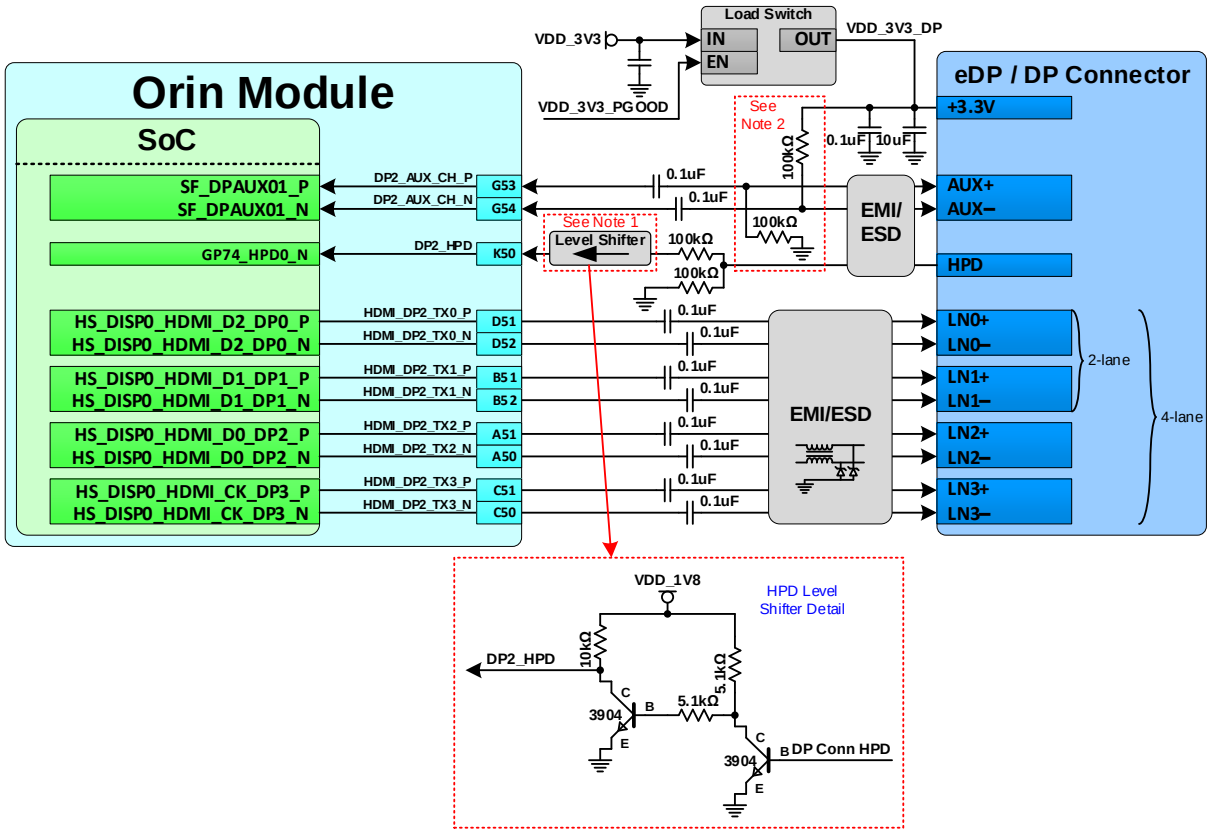
Notes:

1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. The direction shown in this table for DPx_HPD is true when used for Hot-plug Detect. Otherwise, if used as GPIOs, the direction is bidirectional.

9.1 DP and eDP

Figure 9-1 shows a basic connection example to DP or eDP connectors.

Figure 9-1. DP and eDP Connection Example

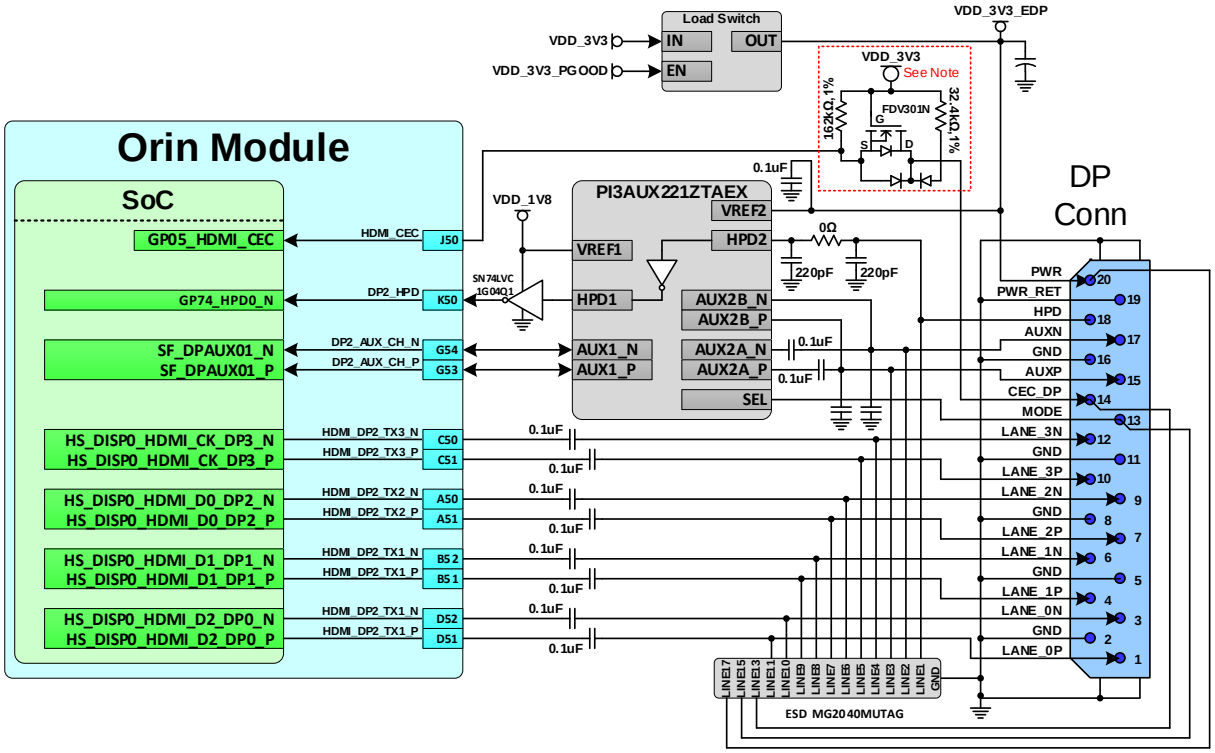


Notes:

1. A Level shifter is required on HPD to avoid the pin from being driven when the module is off. The level shifter must be non-inverting (preserve polarity of the signal from the display). See level shifter detail below main figure.
2. Pull-up/down only required for DP - not for eDP.
3. If EMI devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing and electrical requirements of the DisplayPort specification for the modes to be supported. Any ESD solution must also maintain signal integrity and meet the DisplayPort requirements for the modes to be supported.

Figure 9-2 shows an example connection to a DP connector using an integrated PIAUX221 device to reduce the components required for level shifting and pull-up resistors. This design also supports DP++ and CEC (optional).

Figure 9-2. DP Connection Example w/Integrated PI3AUX221 Device



Notes:

1. CEC is optional. If not required, the circuit shown can be removed and the CEC_DP pin on the DP connector (Pin 14) should have a weak pulldown (5.1MΩ used in reference design)
2. If EMI devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing and electrical requirements of the DisplayPort specification for the modes to be supported. Any ESD solution must also maintain signal integrity and meet the DisplayPort requirements for the modes to be supported.

Table 9-2. Basic DP and eDP Signal Connections

Module Pin Name	Type	Termination	Description
HDMI_DP2_TX[3:0]_P/N	O	Series 0.1uF capacitors on all lines	DP/eDP Differential Data Lanes: Connect to matching pins on display connector. See DP/HDMI Pin Descriptions and connection diagram for details.
DP2_AUX_CH_P/N	I/OD	Series 0.1uF capacitors DP2_AUX_CH_P pulled to GND through 100kΩ resistor. DP2_AUX_CH_N pulled to VDD_3V3_DP through 100kΩ resistor.	DP/eDP: Auxiliary Channels: Connect to AUX_CH+/– on display connector.
DP2_HPD	I	100kΩ series resistor and 100kΩ resistor to GND then Level shifter (non-inverting) between connector and module pin.	DP/eDP: Hot Plug Detect: Connect to HPD pin on display connector. See Connections Example figure for details.
VDD_3V3_EDP	P	From level shifter	DP/eDP 3.3V supply: Connect output of load switch to DP/eDP connector +3.3V pin. Connect input of load switch to VDD_3V3. Connect enable of load switch to VDD_3V3_PGOOD.

Table 9-3. DP Signal Connections for integrated PI3AUX221 Solution

Module Pin Name (Other)	Type	Termination	Description
HDMI_DP2_TX[3:0]_N/P	O	Series 0.1uF capacitors on all lines. Optional ESD to GND.	DP/eDP Differential Data Lanes: Connect to matching pins on display connector.
DP2_AUX_CH_N/P	I/OD	To PI3AUX221 with 0.1uF series capacitors on AUX2A_N/P path to connector.	DP Auxiliary Channel: Connect to PI3AUX221 device to AUX1_N/P pins. Connect PI3xxx device AUX2B_N/P pins to AUX_CH–/P pins on DP connector. Connect PI3xxx device AUX2A_N/P pins through series AC capacitors to AUX_CH–/P pins on DP connector.
DP2_HPD	I	To PI3AUX221 through inverter then to DP connector HPD pin.	DP Hot Plug Detect: Connect to inverter output then HPD1 pin of PI3AUX221 device. Connect PI3xxx HPD2 pin to HPD pin on display connector.
HDMI_CEC	I/OD	Gating circuitry.	Consumer Electronics Control (optional): Connect to CEC_DP pin on DP Connector through circuitry. See details under connection figure or reference design for details.
VDD_3V3_EDP	P	From level shifter	DP 3.3V supply: Connect output of load switch to DP connector +3.3V pin. Connect input of load switch to VDD_3V3. Connect enable of load switch to VDD_3V3_PGOOD.
(PI3AUX221 VREF1)	P		PI3AUX221 Voltage Reference 1: Connect to VDD_1V8.
(PI3AUX221 VREF2)	P		PI3AUX221 Voltage Reference 2: Connect to VDD_3V3_DP.
(PI3AUX221 SEL)	I		PI3AUX221 Mode Select: Connect to MODE pin of DP connector.

9.1.1 DP and eDP Routing Guidelines

Figure 9-3 shows the topology for DisplayPort and embedded DisplayPort. The figure below shows the signal routing requirements including DP_AUX.

Figure 9-3. DP and eDP Differential Main Link Topology

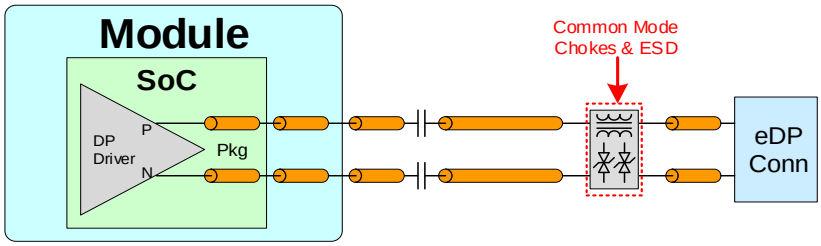
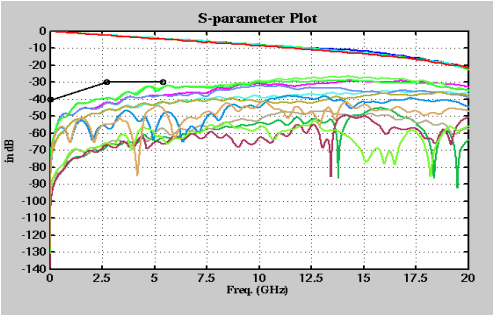
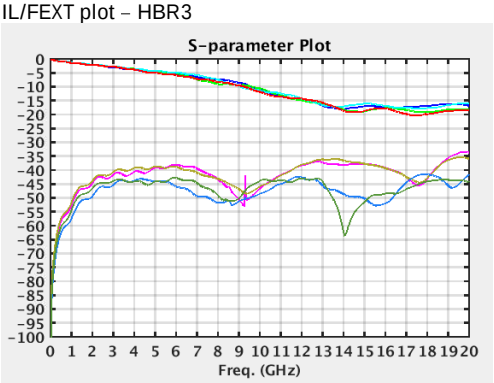
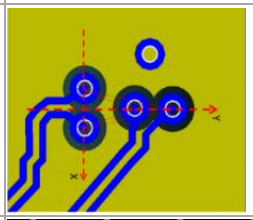
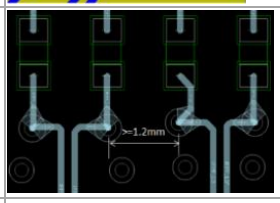


Table 9-4. DP and eDP Main Link Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Max Data Rate / Min UI			Per data lane
HBR3	8.1 / 123	Gbps / ps	
HBR2	5.4 / 185		
HBR	2.7 / 370		
RBR	1.62 / 617		
Number of Loads / Topology	1	load	Point-Point, Differential, Unidirectional
Termination	100	Ω	On die at TX/RX
Electrical Specification			
Insertion Loss			
E-HBR @ 0.675GHz	<=0.7	dB	
PBR 0.68GHz	<=0.7		
HBR 1.35GHz	<=1.2		
HBR2 @ 2.7GHz	<=4.5		
HBR3 @ 4.05GHz	<=5.5		
Resonance dip frequency			
HBR2	>8	GHz	
HBR3	>12		
TDR dip	>85	Ω	@ Tr-200ps (10%-90%)

Parameter	Requirement	Units	Notes
FEXT @ DC @ 2.7GHz @ 5.4GHz	 <= -40dB <= -30dB <= -30dB	IL/FEXT plot – up to HBR2  IL/FEXT plot – HBR3  	
Impedance			
Trace Impedance (Diff pair)	100 90 85	Ω (±10%)	100Ω is the spec. target. 95/85Ω are implementation options (Zdiff does not account for trace coupling) 95Ω should be used to support DP-HDMI co-layout as HDMI 2.0 requires 100Ω impedance (see HDMI section for addition of series resistor Rs). 85Ω can be used if eDP/DP only and is preferable as it provides better trace loss characteristic performance. See Note 1.
Reference Plane	**GND**		
Trace Length (delay), Spacing and Skew			
Trace loss characteristic HBR2 or lower (@ 2.7GHz) HBR3 (@405GHz)	 < 0.64 <=0.9	dB/in	The following max length (delay) is derived based on this characteristic. The length (delay) constraint must be re-defined if loss characteristic is changed.
Max PCB Via dist. from module conn. **RBR/HBR** **HBR2 and HBR3**	 No requirement 7.62	mm	

Parameter	Requirement	Units	Notes
Max trace length (delay) from module to connector			6.9ps/mm assumption for Stripline, 5.9ps/mm for Microstrip.
RBR/HBR			
Stripline	215 (1137.5)	mm (ps)	
Microstrip	215 (975)		
HBR2			
Stripline	184 (1260)		
Microstrip	178 (1050)		
HBR3			
Stripline	162 (1120)		
Microstrip	155 (900)		
Trace spacing (Pair-Pair)			
Stripline	3x	dielectric height	
Microstrip (**HBR/RBR**)	4x		
Microstrip (**HBR2/HBR3**)	5x to 7x		
Trace spacing (Main Link to AUX): Stripline/Microstrip	3x / 5x	dielectric height	
Max Intra-pair (within pair) Skew	0.15 (1)	mm (ps)	Do not perform length (delay) matching within breakout region. Do trace length (delay) matching before hitting discontinuity (i.e. matching to <1ps before the vias or any discontinuity to minimize common mode conversion).
Max Inter-pair (pair-pair) Skew	150	ps	
Via			
Max GND transition Via distance	< 1x	diff pair pitch	For signals switching reference layers, add symmetrical GND stitching Via near signal Vias.
Impedance dip	≥97 ≥92	Ω @ 200ps Ω @ 35ps	The via dimension must be required for the HDMI-DP co-layout condition.
Recommended via dimension for impedance control			
Drill/Pad	200/400	um	
Antipad	>840	um	
Via pitch	≥880	um	
Topology	Y-pattern is recommended keep symmetry Xtalk suppression is best using the Y-pattern. It can also reduce the limit of pair-pair distance.		
	For in-line via, the distance from a via of one lane to the adjacent via from another lane >= 1.2 mm center-center.		
GND via	Place GND via as symmetrically as possible to data pair vias. Up to 4 signal vias (2 diff pairs) can share a single GND return via		GND via is used to maintain return path, while its Xtalk suppression is limited

Parameter	Requirement	Units	Notes
Max # of Vias PTH vias Micro Vias	 4 if all vias are PTH via Not limited as long as total channel loss meets IL spec		
Max Via Stub Length	0.4	mm	
AC Cap			
Value	0.1	uF	Discrete 0402
Max Dist. from AC cap to connector RBR/HBR HBR2/HBR3	 No requirement 0.5	in	
Voiding RBR/HBR HBR2/HBR3	 No requirement Voiding required		**HBR2**: Voiding the plane directly under the pad ~0.1mm larger than the pad size is recommended.
Serpentine (See USB 3.2 Guidelines)			
Connector			
Voiding RBR/HBR HBR2/HBR3	 No requirement Voiding required		HBR2: Standard DP Connector: Voiding requirement is stack-up dependent. For typical stack-ups, voiding on the layer under the connector pad is required to be 5.7mil larger than the connector pad.
General			
Keep critical PCIe traces away from other signal traces or unrelated power traces/areas or power supply components			

Notes:

1. For eDP/DP, the spec puts a higher priority on the trace loss characteristic than on the impedance. However, before selecting 85Ω for impedance, it is important to make sure the selected stack-up, material and trace dimension can achieve the needed low loss characteristic.
2. The average of the differential signals is used for length/delay matching.
3. Do not perform length/delay matching within breakout region. Recommend doing trace length/delay matching to <1ps before vias or any discontinuity to minimize common mode conversion

Table 9-5. Recommended DP and eDP Test Points for Initial Boards

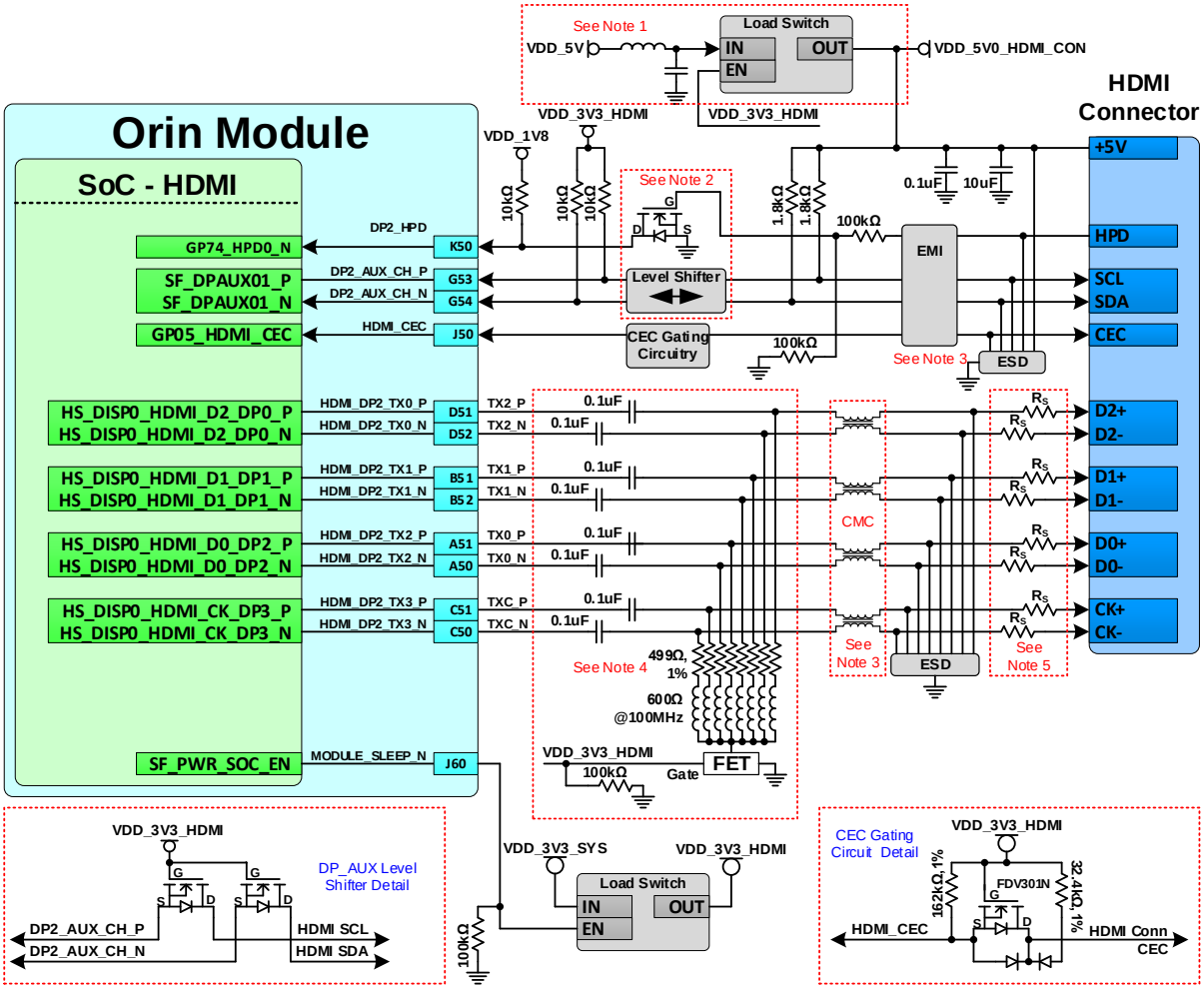
Test Points Recommended	Location
One for each signal line.	Near display connector. Connector pins can be used if accessible.

Note: Test points must be done carefully to minimize signal integrity impact. Avoid stubs and keep pads small and near signal traces

9.2 HDMI

Figure 9-4 shows the connection example for an HDMI connector.

Figure 9-4. HDMI Connection Example



Notes:

1. Load switch circuit is intended to remove power to the HDMI connector, etc. to avoid backdrive on signals to the module. Other mechanisms may be used but must prevent module pins being driven when the module is off.
2. Level shifters required on DDC/HPD. Orin module pads are not 5V tolerant and cannot directly meet HDMI VIL/VIH requirements. HPD level shifter can be non-inverting or inverting.
3. If EMI/ESD devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing and electrical requirements of the HDMI specification for the modes to be supported. See requirements and recommendations in the related sections of Table 9-7.
4. HDMI_DP2_TXx pads are native DP pads and require series AC capacitors and pull-downs to be HDMI compliant. The 499Ω, 1% pull-downs must be disabled when SoC is off to meet the HDMI VOFF requirement. The FET enables the pull-downs when the HDMI interface is to be used. Chokes between pull-downs and FET are required for Standard Technology designs and recommended for HDI designs.
5. See the RS section of Table 9-7.

Table 9-6. HDMI Signal Connections

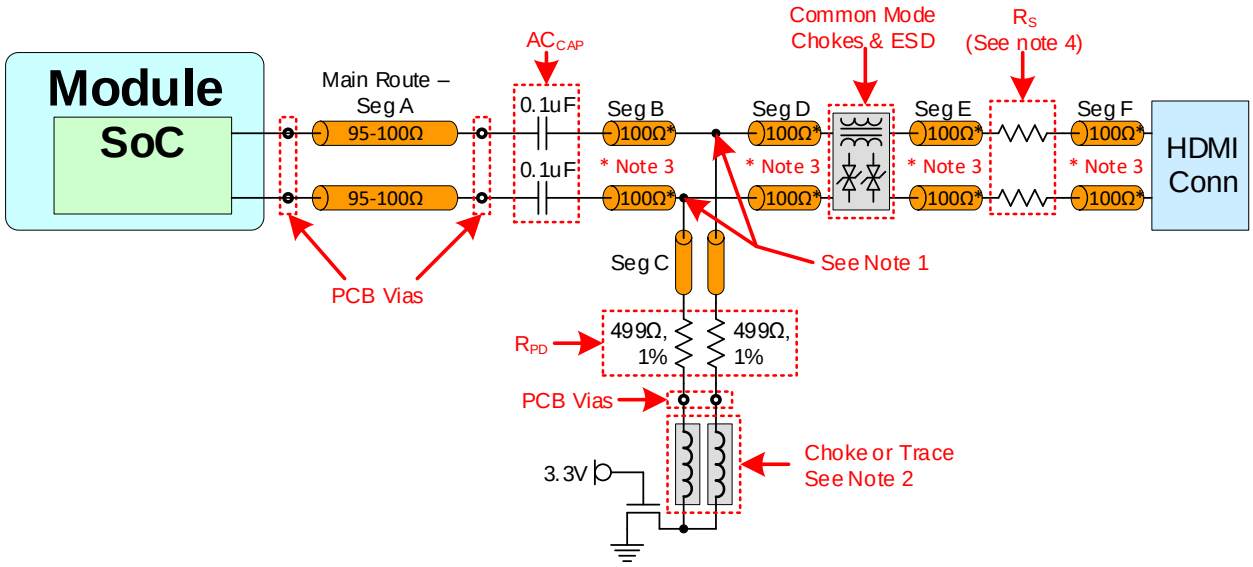
Module Pin Name	Type	Termination (See Note on ESD)	Description
HDMI_DP2_TX3_N/P	DIFF OUT	0.1uF series AC_{CAP} → 500Ω to GND (R_{PD}) (controlled by FET) → EMI/ESD (if required), then ≤6Ω series resistor (R_S, if required).	HDMI Differential Clock: Connect to C−/C+ and pins on HDMI connector
HDMI_DP2_TX[2:0]_N/P	DIFF OUT		HDMI Differential Data: Connect to D[2:0]+/− pins. See Table 9-1 and connection diagram.
DP2_HPD	I	Orin module to Connector: 10kΩ PU to 1.8V → level shifter → 100kΩ series resistor. 100kΩ to GND on connector side.	HDMI Hot Plug Detect: Connect to HPD pin on HDMI Connector
HDMI_CEC	I/OD	Gating circuitry. See details under connection figure or reference design for details.	HDMI Consumer Electronics Control: Connect to CEC on HDMI Connector through circuitry.
DP2_AUX_CH_N/P	I/OD	From Orin module to Connector: 10kΩ PU to 3.3V → level shifter → 1.8kΩ PU to 5V → connector pin See details under connection figure for recommended level shifter circuit.	HDMI: DDC Interface – Clock and Data: Connect DPx_AUX_CH+ to SCL and DPx_AUX_CH− to SDA on HDMI connector
HDMI 5V Supply	P	Adequate decoupling (0.1uF and 10uF recommended) on supply near connector.	HDMI 5V supply to connector: Connect to +5V on HDMI connector.

Note: Any ESD and/or EMI solutions must support targeted modes (frequencies).

9.2.1 HDMI Design Guidelines

Figure 9-5 illustrates the HDMI clock and data topology.

Figure 9-5. HDMI CLK and Data Topology

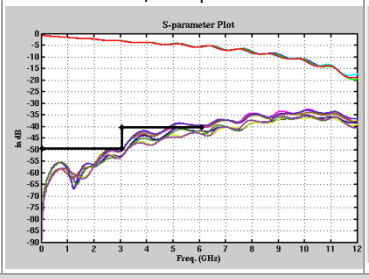
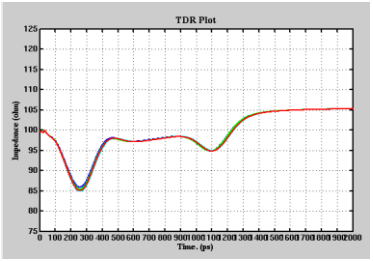


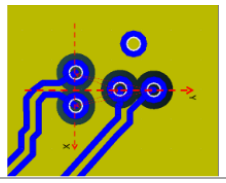
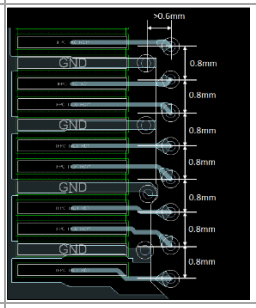
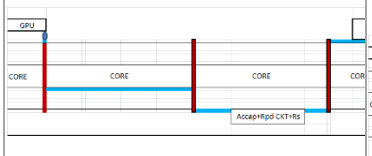
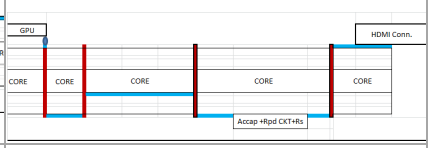
Notes:
1. RPD pad must be on the main trace. RPD and ACCAP must be on same layer.

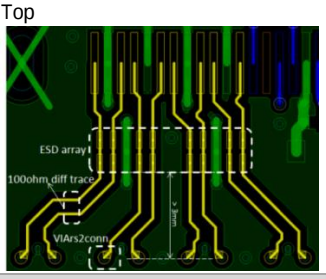
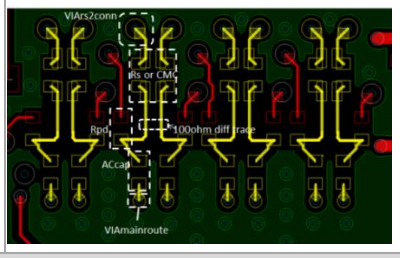
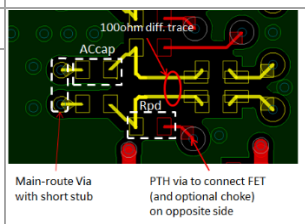
Notes (cont'd):

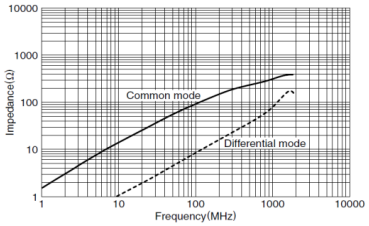
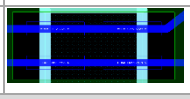
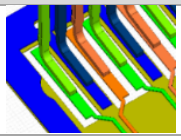
2. Chokes (600 Ω @ 100 MHz) or narrow traces (1 uH@DC-100 MHz) between pull-downs and FET are required for Standard Technology (through-hole) designs and recommended for HDI designs.
3. The trace after the main route via should be routed on the top or bottom layer of the PCB, and either with 100 Ω (for HDMI 2.0 HF 1-9 test) differential impedance, or as uncoupled 50 Ω Single Ended traces.
4. Series resistors (RS) only required to meet HDMI 2.0 compliance. HDMI 2.1 does not require these to meet impedance requirements. See the RS section of Table 9-7 for details.

Table 9-7. HDMI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Electrical Specification			
IL resonance dip frequency	<= 1.7 <= 2 <= 3 < 4.3 > 12	dB @ 1GHz dB @ 1.5GHz dB @ 3GHz dB @ 6GHz GHz	For HDMI 2.0, 6dB & 6GHz is supported.
TDR dip	>= 85	Ω @ Tr=200ps	10%-90%. If TDR dip is 75~85ohm that dip width should < 250ps
FEXT	<= -50 <= -40 <= -40	dB at DC dB at 3GHz dB at 6GHz	
	IL/FEXT plot 		TDR plot 
Impedance			
Trace Impedance Diff pair	100	Ω	±10%. Target is 100Ω. 95Ω for the breakout and main route is an implementation option.
Reference plane	GND		
Trace Length (delay), Spacing and Skew			
Trace loss characteristic:	< 1.1 < 0.8 < 0.4	dB/in. @ 6GHz dB/in. @ 3GHz dB/in. @ 1.5GHz	The max length (delay) is derived based on this characteristic. The length (delay) constraint must be re-defined if the loss characteristic is changed.
Min Trace spacing (Pair-Pair) Stripline: 2.1 Stripline: 1.4b/2.0 Microstrip: 2.1 Microstrip: 1.4b/2.0	 4x 3x 7x 5x to 7x	 dielectric height	For Stripline, this is 3x of the thinner of above and below.
Min Trace spacing (Main Link to DDC) Stripline Microstrip	 3x 5x	dielectric height	For Stripline, this is 3x of the thinner of above and below.

Parameter	Requirement	Units	Notes
Max Total Delay (2.1) Stripline (4x spacing) Microstrip (7x spacing)	 76 (535) 63.5 (375)	mm (ps)	Propagation delay: 6.9ps/mm assumption for Stripline, 5.9ps/mm for Microstrip.
Max Total Delay (1.4b/2.0) Stripline Microstrip (5x spacing) Microstrip (7x spacing)	 101 (700) 88.5 (525) 101 (600)	mm (ps)	Propagation delay: 6.9ps/mm assumption for Stripline, 5.9ps/mm for Microstrip.
Max Intra-Pair (within pair) Skew	0.15 (1)	mm (ps)	See Notes 1, 2 and 3
Max Inter-Pair (pair to pair) Skew	150	ps	See Notes 1, 2 and 3
Max **GND** transition Via distance	1x	Diff pair via pitch	For signals switching reference layers, add one or two ground stitching vias. It is recommended they be symmetrical to signal vias.
Via			
Topology	Y-pattern is recommended keep symmetry		Xtalk suppression is the best by Y-pattern. Also it can reduce the limit of pair-pair distance. Need review (NEXT/FEXT check) if via placement is not Y-pattern. 
Minimum Impedance dip Recommended via dimension for impedance control Drill/Pad Antipad Via pitch	⩾97 ⩾92 200/400 >840 ⩾880	Ω @ 200ps Ω @ 35ps um um um	
GND via	Place GND via as symmetrically as possible to data pair vias. Up to 4 signal vias (2 diff pairs) can share a single GND return via		GND via is used to maintain return path, while its Xtalk suppression is limited
Connector pin via	The break-in trace to the connector pin via should be routed on the BOTTOM in order to avoid via stub effect. Equal spacing (0.8mm) between adjacent signal vias. The x-axis distance between signal and GND via should be > 0.6mm		
Max # of Vias PTH vias Micro Vias	 4 if all vias are PTH via Not limited as long as total channel loss meets IL spec		
	No breakout: ⩽ 3 vias 		breakout on the same layer as main trunk: ⩽ 4 vias 
Max Via Stub Length	0.4	mm	long via stub requires review (IL and resonance dip check)

Parameter	Requirement	Units	Notes
Serpentine (refer to the USB 3.2 Guidelines) Topology (Table 9-6)			
The main-route via dimensions should comply with the via structure rules (See Via section)			
For the connector pin vias, follow the rules for the connector pin vias (See Via section)			
The traces after main-route via should be routed as 100Ω differential or as uncoupled 50ohm Single-ended traces on PCB Top or Bottom.			
Max distance from RPD to main trace (seg B)	1	mm	
Max distance from AC cap to RPD stubbing point (seg A)	~0	mm	
Max distance between ESD and signal via	3	mm	
Add-on Components			
Example of a case where space is limited for placing components.	Top 		Bottom 
AC CAP			
Value	0.1	uF	
Max via distance from BGA	7.62 (52.5)	mm (ps)	
Location	must be placed before pull-down resistor		The distance between the AC cap and the HDMI connector is not restricted.
Placement PTH design Micro-Via design	Place cap on bottom layer if main-route above core Place cap on top layer if main-route below core Not Restricted		
Void	GND (or PWR) void under/above the cap is needed. Void size = SMT area + 1x dielectric height keepout distance		
Pull-down Resistor (RPD), choke/FET			
Value	500	Ω	
Location	Must be placed after AC cap		
Layer of placement	Same layer as AC cap. The FET and choke can be placed on the opposite layer through a PTH via		
Choke between RPD and FET Choke Max Trace Rdc Max Trace length	 600 or 1 ≤20 4	 Ω@100MHz uH@DC-100MHz mΩ mm	Can be choke or Trace. Recommended option for HDMI2.0 HF1-9 improvement.
Void	GND/PWR void under/above cap is preferred		
Common-Mode Choke (Stuffing option – not added unless EMI issue is seen)			

Parameter	Requirement	Units	Notes
Common-mode impedance @ 100MHz Min Max	 65 90	 Ω	TDK ACM2012D-900-2P 
RDC	<=0.3ohm		
Differential TDR impedance	90ohm +/-15% @ Tr=200ps (10%-90%)		
Min Sdd21 @ 2.5GHz	2.22	dB	
Max Scc21 @ 2.5GHz	19.2	dB	
Location	Close to any adjacent discontinuity (< 8mm) – such as connector, via, etc.		
ESD (On-chip protection diode is able to withstand 2kV HMM. External ESD is optional. Designs should include ESD footprint as a stuffing option)			
Max junction capacitance (IO to GND)	0.35	pF	e.g. ON-semiconductor ESD8040
Footprint	Pad right on the net instead of trace stub		 
Location	After pull-down resistor/CMC and before RS		
Void	GND/PWR void under/above the cap is needed. Void size = 1mm x 2mm for 1 pair		
Series Resistor (RS) Series resistor on P/N path for HDMI 2.0 but not required for HDMI 2.1 (Mandatory to meet HDMI 2.0 Compliance.			
Value	⩽ 6	Ω	± 10%. 0ohm is acceptable if the design passes the HDMI2.0 HF1-9 test. Otherwise, adjust the RS value to ensure the HDMI2.0 tests pass: Eye diagram, Vlow test and HF1-9 TDR test
Location	After all components and before HDMI connector		
Void	GND/PWR void under/above the RS device is needed. Void size = SMT area + 1x dielectric height keepout distance.		
Connector			
Connector Voiding	Voiding the ground below the signal lanes 0.1448(5.7mil) larger than the pin itself		

Parameter	Requirement	Units	Notes
General			
Routing over Voids	Routing over voids not allowed except void around device ball/pin the signal is routed to.		
Noise Coupling	Keep critical HDMI related traces including differential clock/data traces and RSET trace away from other signal traces or unrelated power traces/areas or power supply components		

Notes:

1. The average of the differential signals is used for length/delay matching.
2. Do not perform length/delay matching within breakout region. Recommend doing trace length/delay matching to <1ps before vias or any discontinuity to minimize common mode conversion
3. If routing includes a flex or 2nd PCB, the max trace delay and skew calculations must include all the PCBs/flex routing. Solutions with flex/2nd PCB may not achieve maximum frequency operation.

Table 9-8. Recommended HDMI and DP Test Points for Initial Boards

Test Points Recommended	Location
One for each signal line.	Near display connector. Connector pins can be used if accessible.

Note: Test points must be done carefully to maximize integrity. Avoid stubs and keep pads small and near signal traces.

Chapter 10. Video Input

The Orin module supports four MIPI CSI x4 bricks, allowing a variety of device types and combinations to be supported. Up to four quad lane cameras or four dual lane cameras plus two quad lane cameras or six dual lane cameras (total of six in any configuration) are available. Both MIPI D-PHY and C-PHY mode are supported. In D-PHY mode, each data channel has peak bandwidth of up to 2.5 Gbps. For C-PHY, each lane (Trio) supports up to 4.5 Gsps.

Note: Maximum data rate may be limited by use case and memory bandwidth.

Table 10-1. Orin Module CSI Pin Description

Pin #	Module Pin Name	SoC Signal	Usage/Description (See Note 2)	Direction	Pin Type
E42	CSI0_D0_P	HS_CSI0_D0_P	Camera, CSI 0: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
E41	CSI0_D0_N	HS_CSI0_D0_N	Camera, CSI 0: DPHY Data 0–, CPHY Lane 0:B		
F43	CSI0_CLK_P	HS_CSI0_CLK_P	Camera, CSI 0: DPHY Clock+, CPHY Lane 0:C		
F42	CSI0_CLK_N	HS_CSI0_CLK_N	Camera, CSI 0: DPHY Clock–, CPHY Lane 1:C		
E39	CSI0_D1_P	HS_CSI0_D1_P	Camera, CSI 0: DPHY Data 1+, CPHY Lane 1:A		
E38	CSI0_D1_N	HS_CSI0_D1_N	Camera, CSI 0: DPHY Data 1–, CPHY Lane 1:B		
G41	CSI1_D0_P	HS_CSI1_D0_P	Camera, CSI 1: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
G42	CSI1_D0_N	HS_CSI1_D0_N	Camera, CSI 1: DPHY Data 0–, CPHY Lane 0:B		
H43	CSI1_CLK_P	HS_CSI1_CLK_P	Camera, CSI 1: DPHY Clock+, CPHY Lane 0:C		
H42	CSI1_CLK_N	HS_CSI1_CLK_N	Camera, CSI 1: DPHY Clock–, CPHY Lane 1:C		
J41	CSI1_D1_P	HS_CSI1_D1_P	Camera, CSI 1: DPHY Data 1+, CPHY Lane 1:A		
J42	CSI1_D1_N	HS_CSI1_D1_N	Camera, CSI 1: DPHY Data 1–, CPHY Lane 1:B		
A41	CSI2_D0_P	HS_CSI2_D0_P	Camera, CSI 2: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
A42	CSI2_D0_N	HS_CSI2_D0_N	Camera, CSI 2: DPHY Data 0–, CPHY Lane 0:B		
B43	CSI2_CLK_P	HS_CSI2_CLK_P	Camera, CSI 2: DPHY Clock+, CPHY Lane 0:C		
B42	CSI2_CLK_N	HS_CSI2_CLK_N	Camera, CSI 2: DPHY Clock–, CPHY Lane 1:C		
C42	CSI2_D1_P	HS_CSI2_D1_P	Camera, CSI 2: DPHY Data 1+, CPHY Lane 1:A		
C41	CSI2_D1_N	HS_CSI2_D1_N	Camera, CSI 2: DPHY Data 1–, CPHY Lane 1:B		
E45	CSI3_D0_P	HS_CSI3_D0_P	Camera, CSI 3: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
E44	CSI3_D0_N	HS_CSI3_D0_N	Camera, CSI 3: DPHY Data 0–, CPHY Lane 0:B		
F46	CSI3_CLK_P	HS_CSI3_CLK_P	Camera, CSI 3: DPHY Clock+, CPHY Lane 0:C		
F45	CSI3_CLK_N	HS_CSI3_CLK_N	Camera, CSI 3: DPHY Clock–, CPHYLane 1:C		
G44	CSI3_D1_P	HS_CSI3_D1_P	Camera, CSI 3: DPHY Data 1+, CPHY Lane 1:A		

Pin #	Module Pin Name	SoC Signal	Usage/Description (See Note 2)	Direction	Pin Type
G45	CSI3_D1_N	HS_CSI3_D1_N	Camera, CSI 3: DPHY Data 1–, CPHY Lane 1:B		
G48	CSI4_D0_P	HS_CSI4_D0_P	Camera, CSI 4: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
G47	CSI4_D0_N	HS_CSI4_D0_N	Camera, CSI 4: DPHY Data 0–, CPHY Lane 0:B		
F48	CSI4_CLK_P	HS_CSI4_CLK_P	Camera, CSI 4: DPHY Clock+, CPHY Lane 0:C		
F49	CSI4_CLK_N	HS_CSI4_CLK_N	Camera, CSI 4: DPHY Clock–, CPHY Lane 1:C		
E47	CSI4_D1_P	HS_CSI4_D1_P	Camera, CSI 4: DPHY Data 1+, CPHY Lane 1:A		
E48	CSI4_D1_N	HS_CSI4_D1_N	Camera, CSI 4: DPHY Data 1–, CPHY Lane 1:B		
D42	CSI5_D0_P	HS_CSI5_D0_P	Camera, CSI 5: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
D43	CSI5_D0_N	HS_CSI5_D0_N	Camera, CSI 5: DPHY Data 0–, CPHY Lane 0:B		
C44	CSI5_CLK_P	HS_CSI5_CLK_P	Camera, CSI 5: DPHY Clock+, CPHY Lane 0:C		
C45	CSI5_CLK_N	HS_CSI5_CLK_N	Camera, CSI 5: DPHY Clock–, CPHY Lane 1:C		
D46	CSI5_D1_P	HS_CSI5_D1_P	Camera, CSI 5: DPHY Data 1+, CPHY Lane 1:A		
D45	CSI5_D1_N	HS_CSI5_D1_N	Camera, CSI 5: DPHY Data 1–, CPHY Lane 1:B		
K44	CSI6_D0_P	HS_CSI6_D0_P	Camera, CSI 6: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
K43	CSI6_D0_N	HS_CSI6_D0_N	Camera, CSI 6: DPHY Data 0–, CPHY Lane 0:B		
J44	CSI6_CLK_P	HS_CSI6_CLK_P	Camera, CSI 6: DPHY Clock+, CPHY Lane 0:C		
J45	CSI6_CLK_N	HS_CSI6_CLK_N	Camera, CSI 6: DPHY Clock–, CPHY Lane 61:C		
H46	CSI6_D1_P	HS_CSI6_D1_P	Camera, CSI 6: DPHY Data 1+, CPHY Lane 1:A		
H45	CSI6_D1_N	HS_CSI6_D1_N	Camera, CSI 6: DPHY Data 1–, CPHY Lane 1:B		
A44	CSI7_D0_P	HS_CSI7_D0_P	Camera, CSI 7: DPHY Data 0+, CPHY Lane 0:A	Input	MIPI D-PHY/ C-PHY
A45	CSI7_D0_N	HS_CSI7_D0_N	Camera, CSI 7: DPHY Data 0–, CPHY Lane 0:B		
B45	CSI7_CLK_P	HS_CSI7_CLK_P	Camera, CSI 7: DPHY Clock+, CPHY Lane 0:C		
B46	CSI7_CLK_N	HS_CSI7_CLK_N	Camera, CSI 7: DPHY Clock–, CPHY Lane 1:C		
C47	CSI7_D1_P	HS_CSI7_D1_P	Camera, CSI 7: DPHY Data 1+, CPHY Lane 1:A		
C48	CSI7_D1_N	HS_CSI7_D1_N	Camera, CSI 7: DPHY Data 1–, CPHY Lane 1:B		

Notes:

1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. The mapping of CSI CPHY signals inside Orin to the Orin pins is programmable. The default mapping is shown in the figure. Other mappings are possible and may be required in some cases.

Table 10-2. CSI Configurations for D-PHY

Signal Name	x2 Configurations						x4 Configurations			
	#1	#2	#3	#4	#5	#6	#1	#2	#3	#4
CSI_0_D0_P/N	Data						Data			
CSI_0_D1_P/N										
CSI_1_D0_P/N		Data								
CSI_1_D1_P/N										
CSI_2_D0_P/N			Data					Data		
CSI_2_D1_P/N										
CSI_3_D0_P/N				Data						
CSI_3_D1_P/N										
CSI_4_D0_P/N					Data				Data	
CSI_4_D1_P/N										
CSI_5_D0_P/N										
CSI_5_D1_P/N										
CSI_6_D0_P/N						Data				Data
CSI_6_D1_P/N										
CSI_7_D0_P/N										
CSI_7_D1_P/N										
CSI_0_CLK_P/N	Clk						Clk			
CSI_1_CLK_P/N		Clk								
CSI_2_CLK_P/N			Clk					Clk		
CSI_3_CLK_P/N				Clk						
CSI_4_CLK_P/N					Clk				Clk	
CSI_5_CLK_P/N										
CSI_6_CLK_P/N						Clk				Clk
CSI_7_CLK_P/N										

Notes:

1. Each 2-lane option shown in this table can also be used for one single lane camera as well.
2. Combinations of 1, 2 and 4-lane cameras are supported, as long as any 4-lane cameras match one of the four configurations.

Table 10-3. CSI Configurations for C-PHY -x2 and x4

		2-Trio Configs						4-Trio Configs			
Camera # SoC Balls	C-PHY Lanes	#1	#2	#3	#4	#5	#6	#1	#2	#3	#4
CSI_0_CLK_P, CSI_0_D0_P/N	0:0	√						√			
CSI_0_CLK_N, CSI_0_D1_P/N	0:1	√						√			
CSI_1_CLK_P. CSI_1_D0_P/N	1:0		√					√			
CSI_1_CLK_N, CSI_1_D1_P/N	1:1		√					√			
CSI_2_CLK_P, CSI_2_D0_P/N	2:0			√					√		
CSI_2_CLK_N, CSI_2_D1_P/N	2:1			√					√		
CSI_3_CLK_P, CSI_3_D0_P/N	3:0				√				√		
CSI_3_CLK_N, CSI_3_D1_P/N	3:1				√				√		
CSI_4_CLK_P, CSI_4_D0_P/N	4:0					√				√	
CSI_4_CLK_N, CSI_4_D1_P/N	4:1					√				√	
CSI_5_CLK_P, CSI_5_D0_P/N	5:0									√	
CSI_5_CLK_N, CSI_5_D1_P/N	5:1									√	
CSI_6_CLK_P, CSI_6_D0_P/N	6:0						√				√
CSI_6_CLK_N, CSI_6_D1_P/N	6:1						√				√
CSI_7_CLK_P, CSI_7_D0_P/N	7:0										√
CSI_7_CLK_N, CSI_7_D1_P/N	7:1										√

Notes: Each x2 configurations can also be used for one single lane camera (x1 configuration) as well.
Configurations can coexist to support a mix of x1, x2 and x4 lanes, if each signal is not shared between multiple configurations.

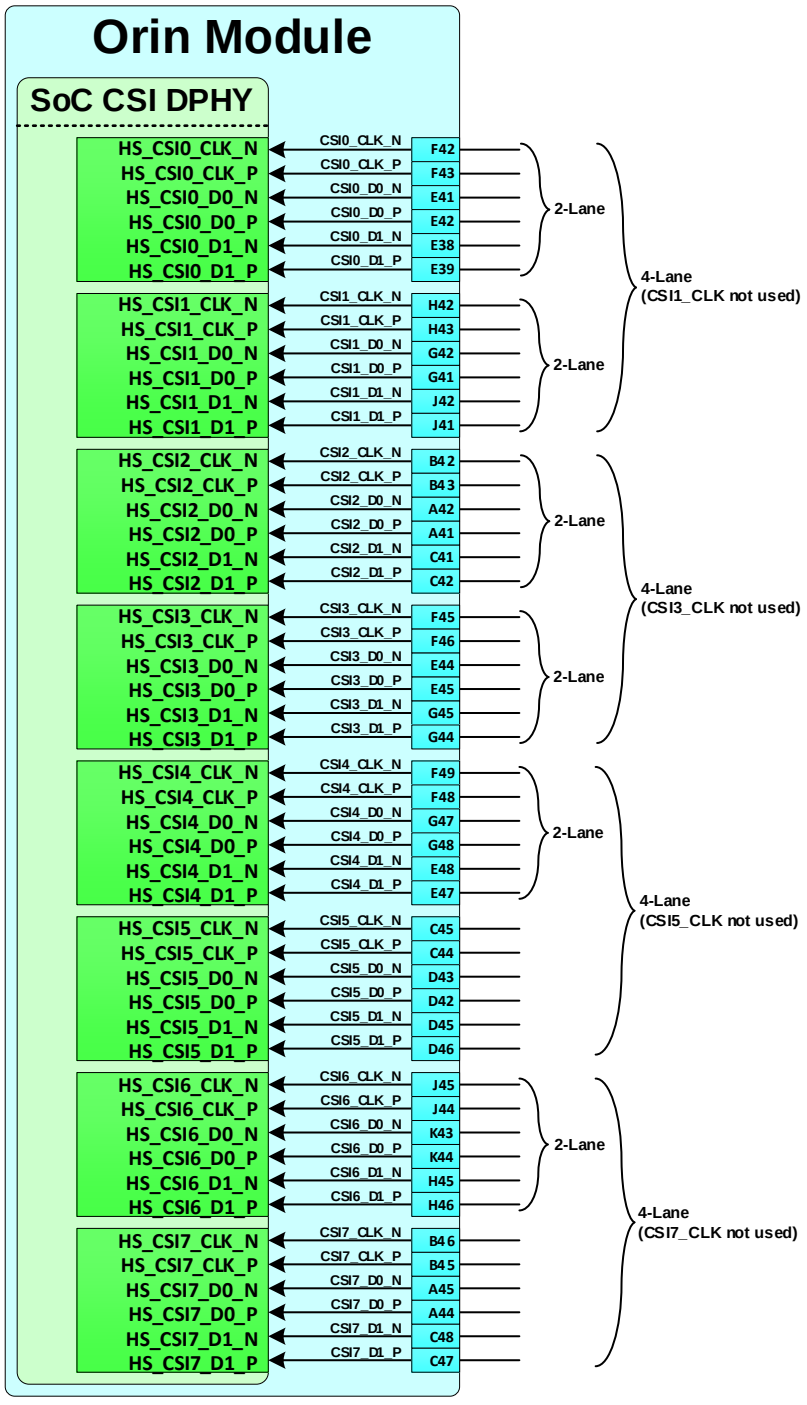
Table 10-4. CSI Configurations C-PHY – x3 and x1

Camera # SoC Balls	x4 Blocks	C-PHY Lanes	#1	#2	#3	#4	#5	#6
CSI_0_CLK_P, CSI_0_D0_P/N	0	0:0	√					
CSI_0_CLK_N, CSI_0_D1_P/N		0:1	√					
CSI_1_CLK_P. CSI_1_D0_P/N		1:0	√					
CSI_1_CLK_N, CSI_1_D1_P/N		1:1		√				
CSI_2_CLK_P, CSI_2_D0_P/N	1	2:0			√			
CSI_2_CLK_N, CSI_2_D1_P/N		2:1			√			
CSI_3_CLK_P, CSI_3_D0_P/N		3:0			√			
CSI_3_CLK_N, CSI_3_D1_P/N		3:1				√		
CSI_4_CLK_P, CSI_4_D0_P/N	2	4:0					√	
CSI_4_CLK_N, CSI_4_D1_P/N		4:1					√	

Camera # SoC Balls	x4 Blocks	C-PHY Lanes	#1	#2	#3	#4	#5	#6
CSI_5_CLK_P, CSI_5_D0_P/N		5:0					√	
CSI_5_CLK_N, CSI_5_D1_P/N		5:1						
CSI_6_CLK_P, CSI_6_D0_P/N	3	6:0						√
CSI_6_CLK_N, CSI_6_D1_P/N		6:1						√
CSI_7_CLK_P, CSI_7_D0_P/N		7:0						√
CSI_7_CLK_N, CSI_7_D1_P/N		7:1						

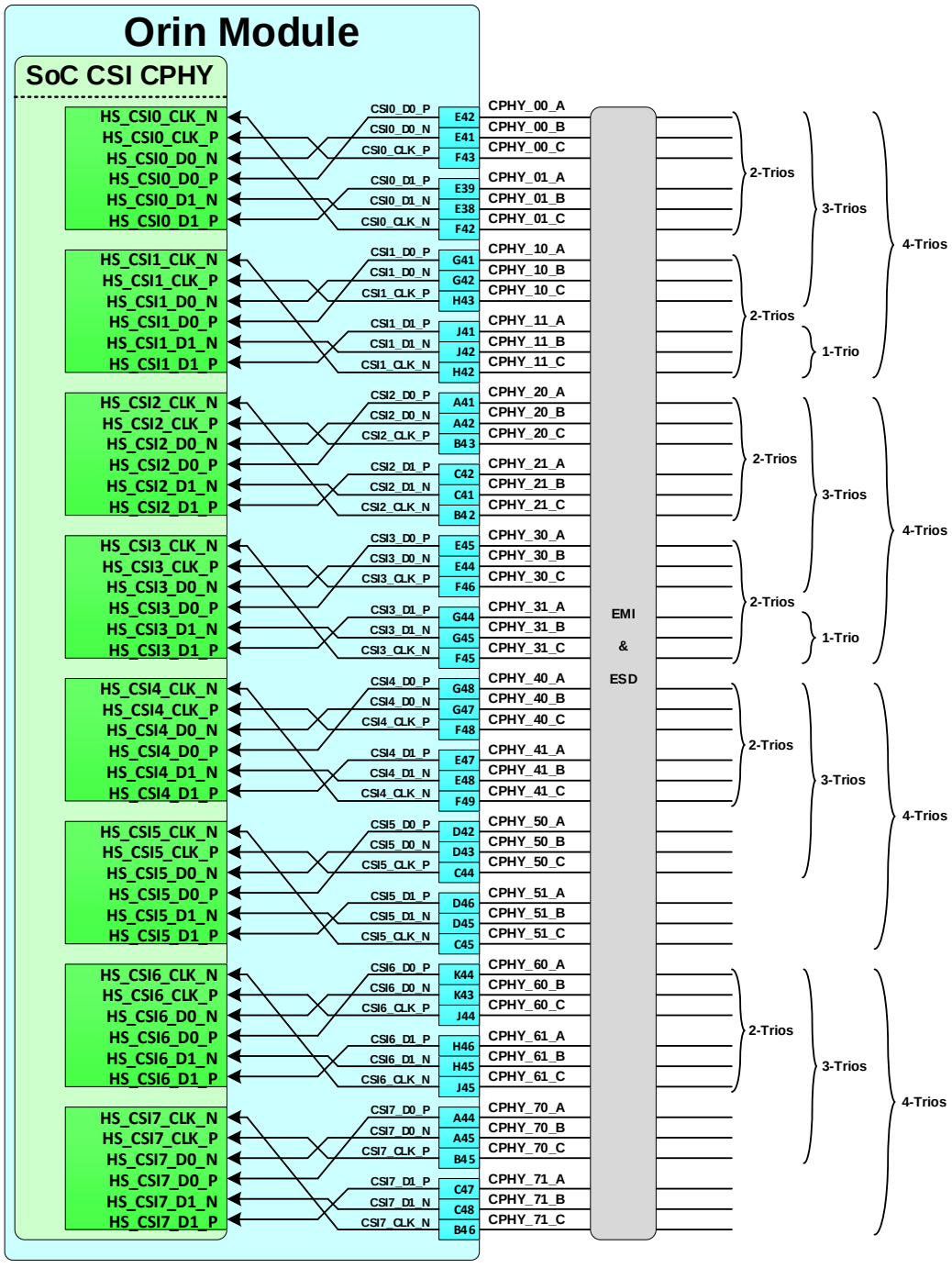
Notes: Each of the above blocks (x4) can be swapped for one of the 2x2 or 1x4 configurations.

Figure 10-1. Camera CSI D-PHY Connections



Note: Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing and Vil/Vih requirements at the receiver and maintain signal quality and meet requirements for the frequencies supported by the design.

Figure 10-2. Camera CSI C-PHY Connections



Notes:

1. The mapping of CSI CPHY signals inside Orin to the Orin pins is programmable. The default mapping is shown in the figure. Other mappings are possible and may be required in some cases.
2. Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing and Vil/Vih requirements at the receiver and maintain signal quality and meet requirements for the frequencies supported by the design.

Table 10-5. MIPI CSI Signal Connections

Module Pin Name	Type	Termination	Description
DPHY Mode			
CSI[7:0]_CLK_N/P	DIFF IN	See note 1	CSI Diff. Clocks: Connect to clock pins of device. See note 2.
CSI[7:0]_D[1:0]_N/P	DIFF IN	See note 1	CSI Diff. Data Lanes: Connect to data pins of device. See note 2.
CPHY Mode			
CSI[7:0]_D0_P (Trio 0, A)	I	See note 1	CSI CPHY Trio 0, A: Connect to matching pin of device. See note 2.
CSI[7:0]_D0_N (Trio 0, B)	I	See note 1	CSI CPHY Trio 0, B: Connect to matching pin of device. See note 2.
CSI[7:0]_CLK_P (Trio 0, C)	I	See note 1	CSI CPHY Trio 0, C: Connect to matching pin of device. See note 2.
CSI[7:0]_D1_P (Trio 1, A)	I	See note 1	CSI CPHY Trio 1, A: Connect to matching pin of device. See note 2.
CSI[7:0]_D1_N (Trio 1, B)	I	See note 1	CSI CPHY Trio 1, B: Connect to matching pin of device. See note 2.
CSI[7:0]_CLK_N (Trio 1, C)	I	See note 1	CSI CPHY Trio 1, C: Connect to matching pin of device. See note 2.

Note:

1. Depending on the mechanical design of the platform and camera modules, ESD protection may be necessary. In addition, EMI control may be needed. Both are shown in the Camera Connection Example diagram. Any EMI/ESD solution must be compatible with the frequency required by the design.
2. See Configurations tables for details.

10.1 CSI D-PHY Design Guidelines

Table 10-6 details the signal routing requirements for CSI D-PHY interface.

Table 10-6. MIPI CSI D-PHY Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate (per data lane) for High-Speed mode Max Frequency (for Low Power mode)	2.5 10	Gbps MHz	
Number of Loads	1	load	
Max Loading (per pin)	**10**	pF	
Reference plane	GND		
Breakout Region Impedance (Single Ended)	45-50	Ω	±15%
Max PCB breakout delay	48	ps	
Trace Impedance Diff pair / Single Ended	90-100 / 45-50	Ω	
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Min Trace spacing	2x	Dielectric height	
Max Insertion loss 1 Gbps / 1.5 Gbps / 2.5 Gbps	 3.10 / 2.96 / 2.17	 dB	
Max trace length (delay) 1 Gbps 1.5 Gbps 2.5 Gbps	 435 (2610) 325 (1953) 170 (1018)	 mm (ps)	
Max Intra-pair Skew	1	ps	See Note 2
Max Trace Delay Skew between DQ and CLK 1 / 1.5 / 2.5 Gbps	 40/26.7/16	 ps	See Note 2

Parameter	Requirement	Units	Notes
Noise Coupling Avoidance	Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components		

Notes:
1. Up to 4 signal vias can share a single GND return via
2. If routing to device includes a flex or 2nd PCB, the max trace and skew calculations must include all the PCBs/flex routing

10.2 CSI C-PHY Design Guidelines

Table 10-7 details the signal routing requirements for CSI C-PHY interface.

Table 10-7. MIPI CSI C-PHY Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate (per trio)	4.5	Gsps	See notes 1 and 2
Topology	Point-Point		With RX Common Mode cap to GND
Termination	Fully ODT (on-die)		50ohms SE to common mode cap
Max Loading (per pin)	**2**	pF	Single ended
Trace Impedance - Single Ended	45-50	Ω	±15%
Reference Plane	GND		
Max PCB breakout Length (Delay)	5 (30)	mm (ps)	
Via proximity (Signal via to GND return via)	< 2	mm	
Min Trace spacing	2.5x	Dielectric height	Recommendation
Inter Trio Trace spacing - Microstrip / Stripline	2x / 3x	Dielectric height	Recommend routing with loosely coupled differential impedance.
Max Insertion loss 4.5 Gsps @ 1.25GHz / 5GHz 3.5 Gsps @ 1.25GHz / 5GHz 2.5 Gsps @ 1.25GHz / 5GHz	 0.97 / 3.92 2.02 / 7.42 2.77 / 7.42	dB	
Max Trace Length total Direct from module conn. to device pins 4.5Gsps 3.5Gsps 2.5Gsps	 63 131 179	mm	It is strongly recommended that designs should be based on the loss guidelines, especially if any connectors are included in the path. The lengths provided are based on EM370 PCB Material with a dB/in loss of 0.393 for 1.25GHz and 1.036 for 5GHz. See Note 3
Max Intra-Trio Skew (Within Trios)	2	ps	A or B pin to C pin skew.
Max Inter-Trio Skew (between Trios)	55	ps	
Routing Layer Restrictions	A trio must route completely on the same layer. For DPHY compatibility, both Trio0 and Trio1 would need to route on the same layer (e.g. D0P/D0N must route on the same layer as CLKP/CLKN and thus so must D1P/D1N).		
Noise Coupling Avoidance	Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components		

Notes:
1. Bit rate in bps is 2.286 * Gsps.
2. Maximum data rate may be limited by use case / memory bandwidth.
3. Note that the max lengths are estimations that do not include the loss from the end device or any connectors between the Orin module connector and the end device. In addition, the effect of via transitions and reflections is not included. Any additional losses (including difference in loss coefficient for PCB material) should be considered and the max length recalculated.

Table 10-8. Recommended CSI Test Points for Initial Boards

Test Points Recommended	Location
One for each signal line.	Near Orin module pins.

Note: Test points must be done carefully to minimize signal integrity impact. Avoid stubs and keep pads small and near signal traces.

Chapter 11. SDIO and SD Card

The Orin module brings a single SDMMC interface to the connector pins for SD card or SDIO use.

Table 11-1. Orin Module SDMMC Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
B6	SDCARD_CLK	GP129_SDMMC_A_CLK	SD Card (or SDIO) Clock	Output	CMOS – 3.3V/1.8V
A5	SDCARD_CMD	GP130_SDMMC_A_CMD	SD Card (or SDIO) Command	Bidir	CMOS – 3.3V/1.8V
E8	SDCARD_D0	GP131_SDMMC_A0	SD Card (or SDIO) Data 0	Bidir	CMOS – 3.3V/1.8V
F8	SDCARD_D1	GP132_SDMMC_A1	SD Card (or SDIO) Data 1	Bidir	CMOS – 3.3V/1.8V
A4	SDCARD_D2	GP133_SDMMC_A2	SD Card (or SDIO) Data 2	Bidir	CMOS – 3.3V/1.8V
D6	SDCARD_D3	GP134_SDMMC_A3	SD Card (or SDIO) Data 3	Bidir	CMOS – 3.3V/1.8V
L6	GPIO02	GP114	GPIO #2 pr SD Card Card Detect	Bidir	CMOS – 1.8V
A7	GPIO29	GP165	GPIO #29, I2S, or SD Card Write Protect	Bidir	CMOS – 1.8V

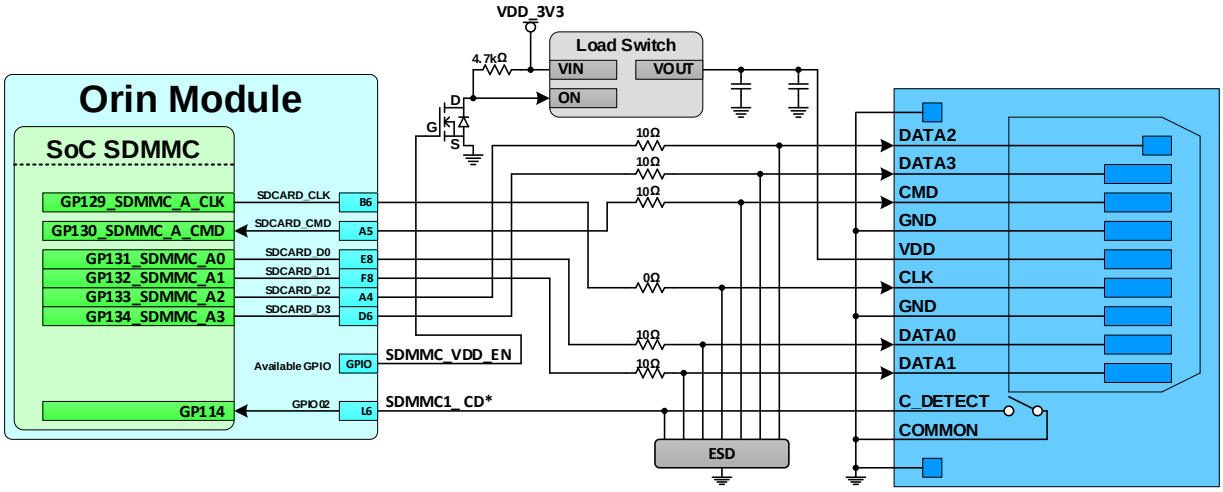
Notes:

1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. The direction shown in the table above for SDCard_CLK is true when used for this function. If used as a GPIO, the pin supports input or output (bidirectional).

11.1 SD Card

Figure 11-1 shows a Micro SD card socket connection example. Internal pull-up resistors are used for SD Card Data and CMD lines. External pull-ups are not required and cannot be used due to the internal pad voltage selection.

Figure 11-1. Micro SD Card Socket Connection Example



Notes:

1. If EMI and/or ESD devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing and Vil/Vih requirements at the receiver and maintain signal quality and meet requirements for the frequencies supported by the design.
2. The supply or load switch for the SD Card VDD must be enabled with a GPIO from Jetson. This is required for correct operation after a warm boot. The GPIO used should be selected so VDD is not powered on by default.
3. Supply (load switch, and so on) used to provide power to the SD Card should be current limited if the supply is shorted to GND.

Table 11-2. SDCARD Signal Connections

Function Signal Name	Type	Termination	Description
SDCARD_CLK	O	See note for EMI/ESD	SDIO/SD Card Clock: Connect to CLK pin of device or socket
SDCARD_CMD	I/O	See note for EMI/ESD	SDIO/SDMMC Command: Connect to CMD pin of device/socket
SDCARD_D[3:0]	I/O		SDIO/SDMMC Data: Connect to Data pins of device or socket
GPIO02 (SDCARD_CD#)	I		SD Card Detect: Connect to CD/C_DETECT pin on socket if required.
GPIO29 (SDCARD_WP)	I		SD Write Protect: Connect to WP pin on SD Card socket.

Note: EMI/ESD may be required for SDIO when used as the SD Card socket interface. Any EMI/ESD device used must be able to meet signal timing/quality requirements.

11.1 SDCARD Design Guidelines

Table 11-3 descripts the routing requirements SD card and SDIO interfaces.

Table 11-3. SD Card and SDIO Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency 3.3V Signaling DS HS Max Frequency 1.8V Signaling SDR12 SDR25 SDR50 SDR104 DDR50	 25 (12.5) 50 (25) 25 (12.5) 50 (25) 100 (50) 208 (104) 50 (50)	MHz (MB/s)	See Note 1
Topology	Point to point		
Reference plane	GND or PWR		See Note 2
Trace Impedance	50	Ω	±15%. 45Ω optional depending on stack-up
Max Via Count PTH HDI	 4 10		 Independant of stackup layers Depends on stackup layers
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	Up to 4 signal Vias can share 1 GND return Via
Trace spacing – Microstrip / Stripline	4x / 3x	dielectric height	
Max Trace length (delay) SDR50 / SDR25 / SDR12 / HS / DS SDR104 / DDR50	 150 (945) 71 (445)	 mm (ps)	
Max Trace Delay Skew in/between CLK and CMD/DAT SDR50 / SDR25 / SDR12 / HS / DS SDR104 / DDR50	 15.9 (100) 3.2 (20)	 mm (ps)	See Note 3
Noise Coupling Avoidance	Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components		

Notes:

1. Actual frequencies may be lower due to clock source/divider limitations.
2. If PWR, 0.01uF decoupling cap required for return current.
3. If routing to SD Card socket includes a flex or 2nd PCB, max trace and skew calculations must include PCB and flex routing.

Table 11-4. SD Card Loading vs. Drive Type

General SD Card Compliance	Parameter	Value	Units	Notes
C_{CARD} (C_{DIE}+C_{PKG})	Min	5	pF	Spec best case value
	Max	10	pF	Spec worst case value
Drive Type	A	33	Ω	UHS50 Card = optional, UHS104 Card = mandatory
	B	50	Ω	UHS50 Card = mandatory, UHS104 Card = mandatory
	C	66	Ω	UHS50 Card = optional, UHS104 Card = mandatory
	D	100	Ω	UHS50 Card = optional, UHS104 Card = mandatory
F_{MAX} (CLK base frequency)	SDR104	208	MHz	Single data rate up to 104MB/sec
	DDR50	50	MHz	Double data rate up to 50MB/sec
	SDR50	100	MHz	Single data rate up to 50MB/sec
	SDR25	50	MHz	Single data rate up to 25MB/sec
	SDR12	25	MHz	Single data rate up to 12.5MB/sec
	HS	50	MHz	Single data rate up to 25MB/sec
	DS	25	MHz	Single data rate up to 12.5MB/sec
C_{LOAD} (C_{CARD}+C_{EQ}) (CLK freq = 208MHz)	Drive Type = A	21	pF	Total load capacitance supported
	Drive Type = B	15	pF	Total load capacitance supported
	Drive Type = C	11	pF	Total load capacitance supported
	Drive Type = D	22	pF	Possibly 22pF+ depending on host system
C_{LOAD} (C_{CARD}+C_{EQ}) (CLK freq = 100/50/25MHz)	Drive Type = A	43	pF	Total load capacitance supported
	Drive Type = B	30	pF	Total load capacitance supported
	Drive Type = C	23	pF	Total load capacitance supported
	Drive Type = D	22	pF	Possibly 22pF+ depending on host system

Table 11-5. Recommended SDCARD Test Points for Initial Boards

Test Points Recommended	Location
One for **SDCARD_CLK** line	Near Device/Connector pin. SD connector pin can be used for device end if accessible.
One SDCARD_Dx line and one for SDCARD_CMD	Near Orin module and Device pins. SD connector pin can be used for device end if accessible.

Chapter 12. Audio

The Orin module brings several PDM and I2S audio interfaces to the module pins and includes a flexible audio-port switching architecture. In addition, digital microphone and speaker interfaces are supported.

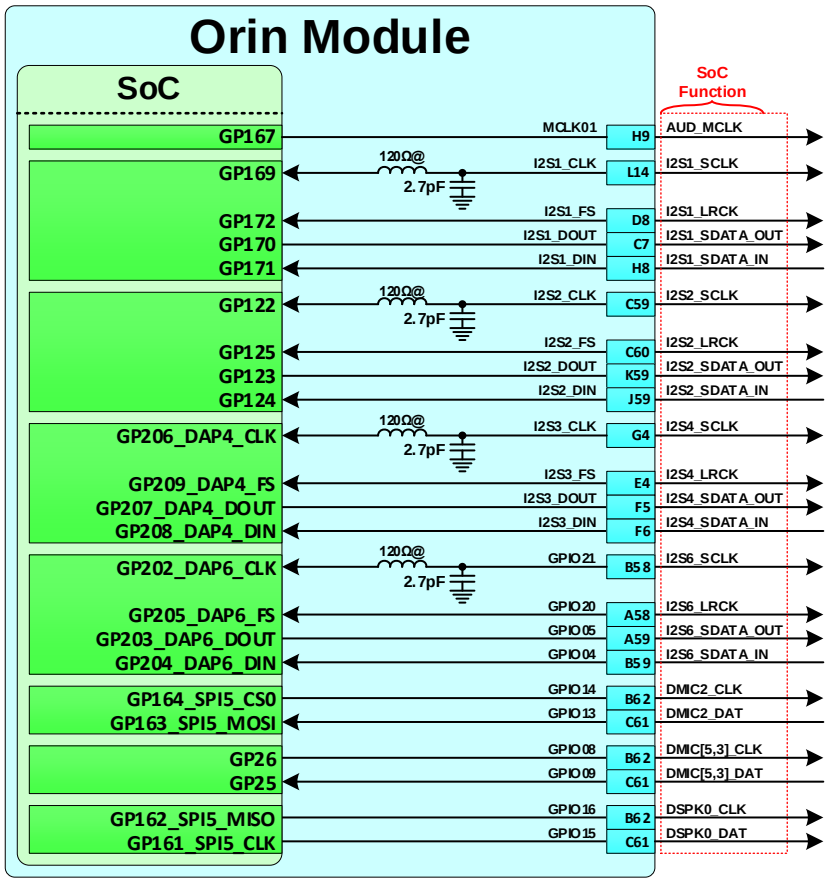
Table 12-1. Orin Module Audio Pin Description

Pin #	Module Pin Name (SoC Audio Function)	SoC Signal	Usage/Description	Direction	Pin Type
H9	MCLK01	GP167	Audio Codec Reference Clock	Output	CMOS – 1.8V
L14	I2S1_CLK	GP169	I2S Audio Port 1 Clock	Bidir	CMOS – 1.8V
D8	I2S1_FS	GP172	I2S Audio Port 1 Left/Right Clock	Bidir	
C7	I2S1_SDOUT	GP170	I2S Audio Port 1 Data Out	Output	
H8	I2S1_SDIN	GP171	I2S Audio Port 1 Data In	Input	
G4	I2S2_CLK	GP122	I2S Audio Port 2 Clock	Bidir	CMOS – 1.8V
E4	I2S2_FS	GP125	I2S Audio Port 2 Left/Right Clock	Bidir	
F5	I2S2_DOUT	GP123	I2S Audio Port 2 Data Out	Output	
F6	I2S2_DIN	GP124	I2S Audio Port 2 Data In	Input	
C59	I2S3_SCLK	GP206_DAP4_CLK	I2S Audio Port 3 Clock	Bidir	CMOS – 1.8V
C60	I2S3_FS	GP209_DAP4_FS	I2S Audio Port 3 Left/Right Clock	Bidir	
K59	I2S3_DOUT	GP207_DAP4_DOUT	I2S Audio Port 3 Data Out	Output	
J59	I2S3_DIN	GP208_DAP4_DIN	I2S Audio Port 3 Data In	Input	
B58	GPIO21 (I2S6_SCLK)	GP202_DAP6_CLK	I2S Audio Port 6 Clock	Bidir	CMOS – 1.8V
A58	GPIO20 (I2S6_LRCK)	GP205_DAP6_FS	I2S Audio Port 6 Left/Right Clock	Bidir	
A59	GPIO05 (I2S6_SDOUT)	GP203_DAP6_DOUT	I2S Audio Port 6 Data Out	Output	
B59	GPIO04 (I2S6_SDIN)	GP204_DAP6_DIN	I2S Audio Port 6 Data In	Input	
L15	GPIO14 (DMIC2_CLK)	GP164_SPI5_CS0	Digital Mic Input 2 Clock	Output	CMOS – 1.8V
G7	GPIO13 (DMIC2_DAT)	GP163_SPI5_MOSI	Digital Mic Input 2 Data	Input	
C61	GPIO09 (DMIC3/5_CLK)	GP25	Digital Mic Input 3/5Clock	Output	CMOS – 3.3V
B62	GPIO08 (DMIC3/5_DAT)	GP26	Digital Mic Input 3/5 Data	Input	
F9	GPIO16 (DSPK0_CLK)	GP162_SPI5_MISO	Digital Speaker Output 2 Clock	Output	CMOS – 1.8V
F10	GPIO15 (DSPK0_DAT)	GP161_SPI5_CLK	Digital Speaker Output 2 Data	Output	

Notes:

1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. The direction indicated for MCLKx, I2Sx, and GPIOx are associated with their use as I2S or MCLK signals. The pins support GPIO functionality, so support both input and output operation (bidirectional).

Figure 12-1. Audio Device Connections



Notes:

1. The I2S interfaces can be used in either Initiator or target mode.
2. A capacitor from I2Sn_FS to GND should be included if SoC is an I2S target and the edge_cntrl configuration = 1 (SDATA driven on positive edge of CLK). The value of the capacitor should be chosen to provide a minimum of 2ns hold time for the I2Sn_FS edge after the rising edge of I2Sn_CLK.

Table 12-2. Audio Interface Signal Connections

Module Pin Name (Orin Function)	Type	Termination	Description
I2Sx_CLK (I2Sx_SCLK)	I/O	120Ω Bead in series and 2.7pF capacitor to GND (on Orin module).	I2S Serial Clock: Connect to I2S/PDM CLK pin of audio device.
I2Sx_FS (I2Sx_LRCK)	I/O		I2S Left/Right Clock: Connect to Left/Right Clock pin of audio device.
I2Sx_DOUT (I2Sx_SDOUT)	I/O		I2S Data Output: Connect to Data Input pin of audio device.

Module Pin Name (Orin Function)	Type	Termination	Description
I2Sx_DIN (I2Sx_SDIN)	I		I2S Data Input: Connect to Data Output pin of audio device.
(DMICx_CLK)	O		DMIC Clock: Connect to Digital Microphone device clock pin.
(DMICx_DAT)	I		DMIC Data: Connect to Digital Microphone device data pin.
(DSPKx_CLK)	O		DSPK Clock: Connect to Digital Speaker device clock pin.
(DSPKx_DAT)	O		DSPK Data: Connect to Digital Speaker device data pin.
(AUD_MCLK)	O		Audio Codec Reference Clock: Connect to clock pin of Audio Codec.

12.1.1 I2S Design Guidelines

Table 12-3 details the signal routing requirements for the I2S interface.

Table 12-3. I2S Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Configuration / Device Organization	1	load	
Max Loading	8	pF	
Reference plane	GND		
Breakout Region Impedance	Min width/spacing		
Trace Impedance	50	Ω	±20%
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing - Microstrip or Stripline	2x	dielectric height	
Max Trace Delay	3600 (~560)	ps (mm)	
Max Trace Delay Skew between SCLK and SDATA_OUT/IN	250 (40)	ps (mm)	

Note: Up to 4 signal Vias can share a single GND return Via

12.2 DMIC Design Guidelines

Table 12-4 details the signal routing requirements for the DMIC interface.

Table 12-4. DMIC Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Clock Frequency/Period	12/83.33	MHz/ns	
Data Bit-rate/Period (DDR24)	24/41.66	Mbps/ns	
Configuration / Device Organization	1	load	
Topology	Point to Point		
Reference plane	GND		
Trace Impedance	45-50	Ω	±20%
Via proximity (Signal via to GND return via)	< 3.8 (24)	mm (ps)	See Note
Trace spacing – Microstrip / Stripline	2x / 2x	dielectric height	
Max Trace Delay	1280	ps	
Max Trace Delay Skew between CLK and DAT	150	ps	

Note: Up to 4 signal vias can share a single GND return via.

Chapter 13. I2C

The Orin module brings multiple I2C interfaces to the module pins.

Table 13-1. Orin Module I2C Pin Description

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
K5	I2C1_CLK	GP126_I2C1_CLK	General I2C 1 Clock	Bidir	Open-Drain – 1.8V (Back-drive capable to 1.8V)
L8	I2C1_DAT	GP127_I2C1_DAT	General I2C 1 Data		
J61	I2C2_CLK	GP13_I2C2_CLK	General I2C 2 Clock		
K61	I2C2_DAT	GP14_I2C2_DAT	General I2C 2 Data		
F53	I2C3_CLK	GP54_I2C3_CLK	General I2C 3 Clock		
E53	I2C3_DAT	GP55_I2C3_DAT	General I2C 3 Data		
D61	I2C4_CLK	GP15_I2C8_CLK	General I2C 4 Clock		
E60	I2C4_DAT	GP16_I2C8_DAT	General I2C 4 Data		
A53	I2C5_CLK	GP81_I2C9_CLK	General I2C 5 Clock		
C53	I2C5_DAT	GP82_I2C9_DAT	General I2C 5 Data		
J52	DP1_AUX_CH_P	GP75_I2C4_CLK	General I2C 6 Clock		
J53	DP1_AUX_CH_N	GP76_I2C4_DAT	General I2C 6 Data		
F52	DP0_AUX_CH_P	GP78_I2C7_CLK	General I2C 7 Clock		
F51	DP0_AUX_CH_N	GP79_I2C7_DAT	General I2C 7 Data		
G53	DP2_AUX_CH_P	SF_DPAUX01_P	Display Port 2 Aux+ or HDMI DDC SCL. AC-Coupled on Carrier Board for DP AUX (eDP/DP) or pulled high for DDC/I2C.	Bidir	Open-Drain, 1.8V (3.3V tolerant, back-drive capable to 1.8V)
G54	DP2_AUX_CH_N	SF_DPAUX01_N	Display Port 2 Aux– or HDMI DDC SDA. AC-Coupled on Carrier Board for DP AUX (eDP/DP) or pulled high for DDC/I2C.	Bidir	

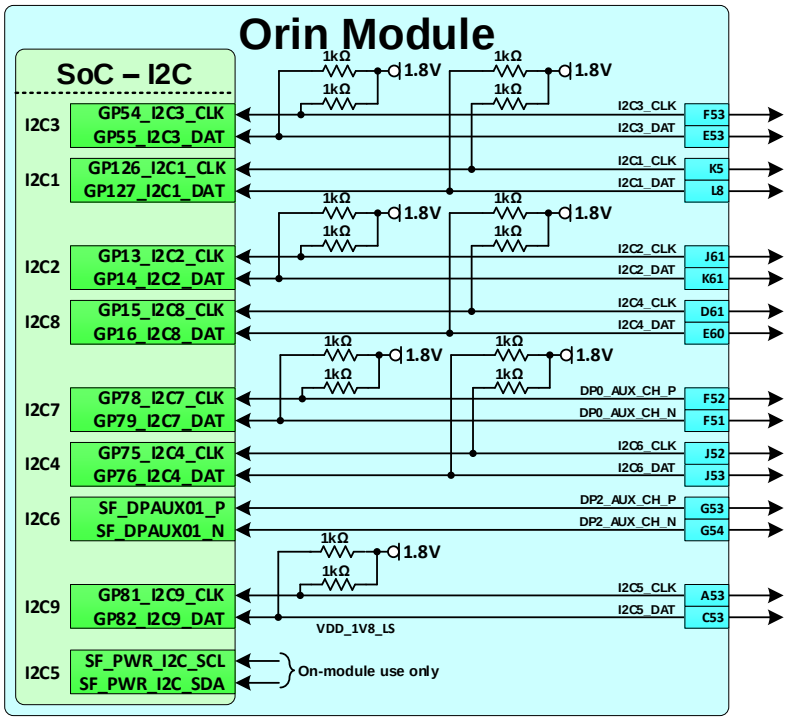
Notes: In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.

Table 13-2. I2C Interface Mapping

Ctrlr	Module Pin Names (Orin Pins)	Usage on Module	Orin Block	On-Module Pull-up/voltage
I2C1	I2C1_CLK/DAT	ID EEPROM (7h50)	J	1KΩ to 1.8V
I2C2	I2C2_CLK/DAT	Power Monitors (7H40 and 7h41)	B_AO	1KΩ to 1.8V (also Power Monitors via level shifter)
I2C3	I2C3_CLK/DAT		F (CAM)	1KΩ to 1.8V
I2C4	DP1_AUX_CH_P/N		G (EDP)	1KΩ to 1.8V
I2C5	(PWR_I2C_SCL/SDA) On-module only	N/A	A_AO (SYS)	N/A
I2C6	DP2_AUX_CH_P/N		G (EDP)	None
I2C7	DP0_AUX_CH_P/N		G (EDP)	1KΩ to 1.8V
I2C8	I2C4_CLK/DAT		B_AO	1KΩ to 1.8V
I2C9	I2C5_CLK/DAT		G (EDP)	1KΩ to 1.8V

Note: The DP2_AUX_CH_P/N pins support either I2C or DP_AUX functionality. DP_AUX is used for DP if this is implemented. HDMI uses the pins for DDC (I2C). Since the I2C and DP_AUX share the same pins, only one can be used in a design.

Figure 13-1. I2C Connections



Notes:

1. For I2C interfaces that have on-module pull-ups to 1.8V, the carrier board should either not have additional pull-ups, or only to 1.8V.
2. Any I2C pull-ups on the carrier board must be connected to power rails that are off when the Orin module is off.
3. If I2C interfaces are routed to M.2 Key E or Key M connectors, it is recommended that 0Ω series resistors be included to allow these to be disconnected. Some M.2 Key E and Key M cards can cause conflicts with other devices connected to the I2C interfaces.

Table 13-3. I2C Signal Connections

Module Pin Name	Type	Termination	Description
I2Cx_CLK/DAT	I/OD	1kΩ pull-ups to 1.8V on module	General I2C Clock\Data. Connect to CLK/Data pins of 1.8V devices
DP0_AUX_CH_P/N	I/OD		I2C Clock (_P) and Data (_N).
DP2_AUX_CH_P/N	I/OD	See eDP/HDMI/DP sections for correct termination	DP_AUX Channel (eDP/DP) or DDC I2C 2 Clock and Data (HDMI). Connect to AUX_CH_P/N (DP) or SCL/SDA (HDMI). Alternately available as I2C IF.

Notes:

1. If some devices require a different voltage level than others connected to the same I2C bus, level shifters are required.
2. For I2C interfaces that are pulled up to 1.8V, disable the E_IO_HV option for these pads. For I2C interfaces that are pulled up to 3.3V, enable the E_IO_HV option. The E_IO_HV option is selected in the Pinmux registers.

13.1.1 I2C Design Guidelines

Care must be taken to ensure I2C peripherals on same I2C bus connected to Orin module do not have duplicate addresses. Addresses can be in two forms: 7-bit, with the Read/Write bit removed or 8-bit including the Read/Write bit.

Make sure I2C device addresses are compared using the same form- all 7-bit or all 8-bit format.

Table 13-4. I2C Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency - Standard-mode / Fm / Fm+	100 / 400 / 1000	kHz	See Note 1
Topology	Single ended, bi-directional, multiple initiators / targets		
Max Loading - Standard-mode / Fm / Fm+	400	pF	Total of all loads
Reference plane	GND or PWR		
Trace Impedance	50 – 60	Ω	±15%
Trace Spacing	1x	dielectric height	
Max Trace Delay Standard Mode Fm and Fm+	 3400 (~500) 1700 (~10)	ps (mm)	

Notes:

1. Fm = Fast-mode, Fm+ = Fast-mode Plus
2. Avoid routing I2C signals near noisy traces, supplies or components such as a switching power regulator.
3. No requirement for decoupling caps for PWR reference

13.1.2 De-bounce

Table 13-5 contains the allowable De-bounce settings for the various I2C modes.

Table 13-5. De-bounce Settings

I2C Mode	Clock Source	Source Clock Freq	I2C Source Divisor	Sm/Fm Divisor	De-bounce Value	I2C SCL Freq
Fm+	PLLP_OUT0	408MHz	5 (0x04)	10 (0x9)	0	1016KHz
					5:1	905.8KHz
					7:6	816KHz
Fm	PLLP_OUT0	408MHz	5 (0x4)	26 (0x19)	7:0	392KHz
Sm	PLLP_OUT0	408MHz	20 (0x13)	26 (0x19)	7:0	98KHz

Note: sm = standard mode

Chapter 14. SPI

Orin module provides multiple Serial Peripheral interfaces (SPI) as listed in Table 14-1. .

Table 14-1. Orin Module SPI Pin Description

Pin #	Module Pin Name (SoC SPI Function)	SoC Signal	Usage/Description	Direction	Pin Type
J57	SPI1_CLK	GP47_SPI1_CLK	SPI 1 Clock	Bidir	CMOS - 1.8V (3.3V tolerant, back-drive capable to 1.8V)
D55	SPI1_MOSI	GP49_SPI1_MOSI	SPI 1 Initiator Out / Target In		
A56	SPI1_MISO	GP48_SPI1_MISO	SPI 1 Initiator In / Target Out		
E55	SPI1_CS0_N	GP50_SPI1_CS0_N	SPI 1 Chip Select 0		
B56	SPI1_CS1_N	GP51_SPI1_CS1_N	SPI 1 Chip Select 1		
E61	SPI2_CLK	GP06_SPI2_CLK	SPI 2 Clock	Bidir	CMOS - 1.8V (3.3V tolerant, back-drive capable to 1.8V)
F60	SPI2_MOSI	GP08_SPI2_MOSI	SPI 2 Initiator Out / Target In		
D62	SPI2_MISO	GP07_SPI2_MISO	SPI 2 Initiator In / Target Out		
D60	SPI2_CS0_N	GP09_SPI2_CS_N	SPI 2 Chip Select 0		
F55	SPI3_CLK	GP36_SPI3_CLK	SPI 3 Clock	Bidir	CMOS - 1.8V (3.3V tolerant, back-drive capable to 1.8V)
G56	SPI3_MOSI	GP38_SPI3_MOSI	SPI 3 Initiator Out / Target In		
D56	SPI3_MISO	GP37_SPI3_MISO	SPI 3 Initiator In / Target Out		
C57	SPI3_CS0_N	GP39_SPI3_CS0_N	SPI 3 Chip Select 0		
E56	SPI3_CS1_N	GP40_SPI3_CS1_N	SPI 3 Chip Select 1		

Notes:

1. The Direction depends on whether Orin is the initiator or target. If Orin is initiator, the clock, chip select and MOSI are outputs and MISO is an input. If Orin is target, the clock, chip select and MOSI are inputs and MISO is an output.
2. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.

Figure 14-1. Orin Module SPI Connections

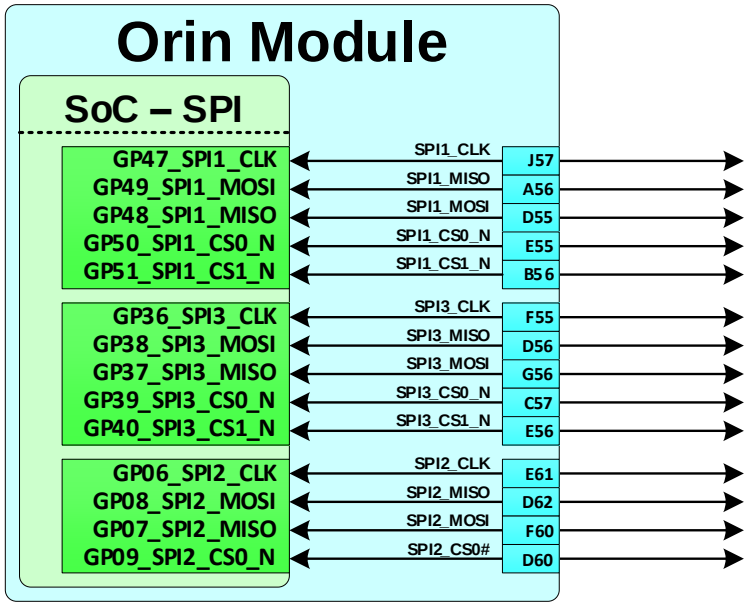


Figure 14-2 shows the basic SPI connections.

Figure 14-2. Basic SPI Connections

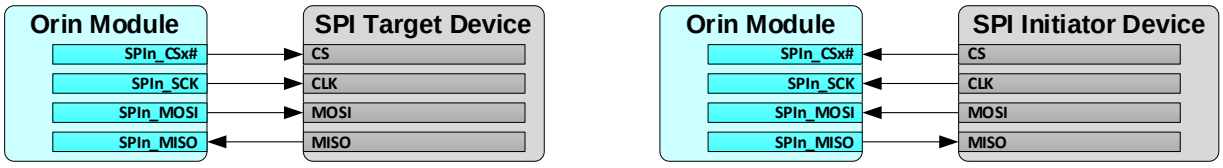


Table 14-2. SPI Signal Connections

Module Pin Names (SoC Function)	Type	Termination	Description
SPIx_CLK	I/O		SPI Clock.: Connect to Peripheral CLK pin(s)
SPIx_MOSI	I/O		SPI Data Output: Connect to Peripheral MOSI pin(s)
SPIx_MISO	I/O		SPI Data Input: Connect to Peripheral MISO pin(s)
SPIx_CS[1:0]_N	I/O		SPI Chip Selects.: Connect one CS_N pin per SPI IF to each target Peripheral CS pin

14.1.1 SPI Design Guidelines

Figure 14-3 shows the SPI topologies.

Figure 14-3. SPI Topologies

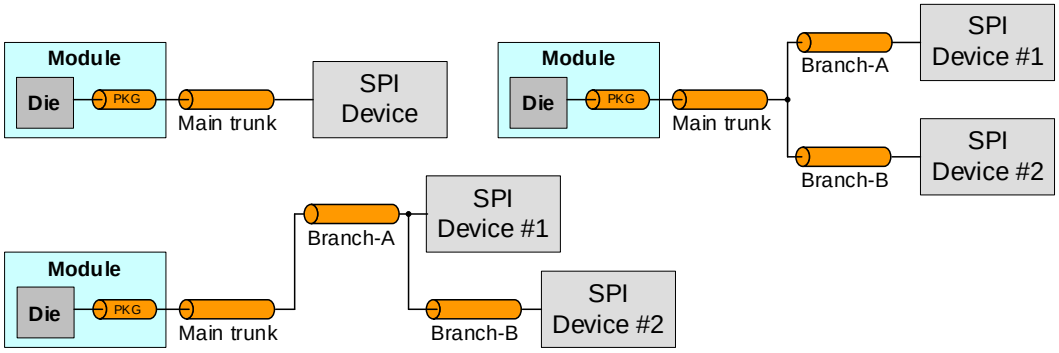


Table 14-3. SPI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency SDR32.5 (SPI devices w/Fmax >50MHz) SDR25 (SPI devices w/Fmax <50MHz) SDR15 (applies to 2-load topologies)	 65 50 30	MHz	
Configuration / Device Organization	3	load	
Max Loading (per pin)	10	pF	
Trace Impedance	45-50	Ω	±15%
Reference plane	GND or PWR		See note 1
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See note 2
Trace spacing - Microstrip / Stripline	3x / 2x	dielectric height	
PCB noise avoidance	3x	dielectric height	
Max PCB breakout delay	6.5 (40)	mm (ps)	
Max Trace Length (Delay) for MOSI, MISO, SCK and CS	109 (685)	mm (ps)	
Max Trace Length (Delay) Skew from MOSI, MISO and CS to SCK	16 (100)	mm (ps)	At any point

Notes:

1. If PWR, add 2x 0201 0.1uF and 2x 0402 4.7uF decoupling capacitors between PWR and GND for return current.
2. Up to 4 signal vias can share a single GND return via.

Table 14-4. Recommended SPI Test Points for Initial Boards

Test Points Recommended	Location
One for each SPI signal line used	Near Orin module and Device pins.

Chapter 15. UART

Orin module brings multiple UARTs out to the main connector as listed in Table 15-1.

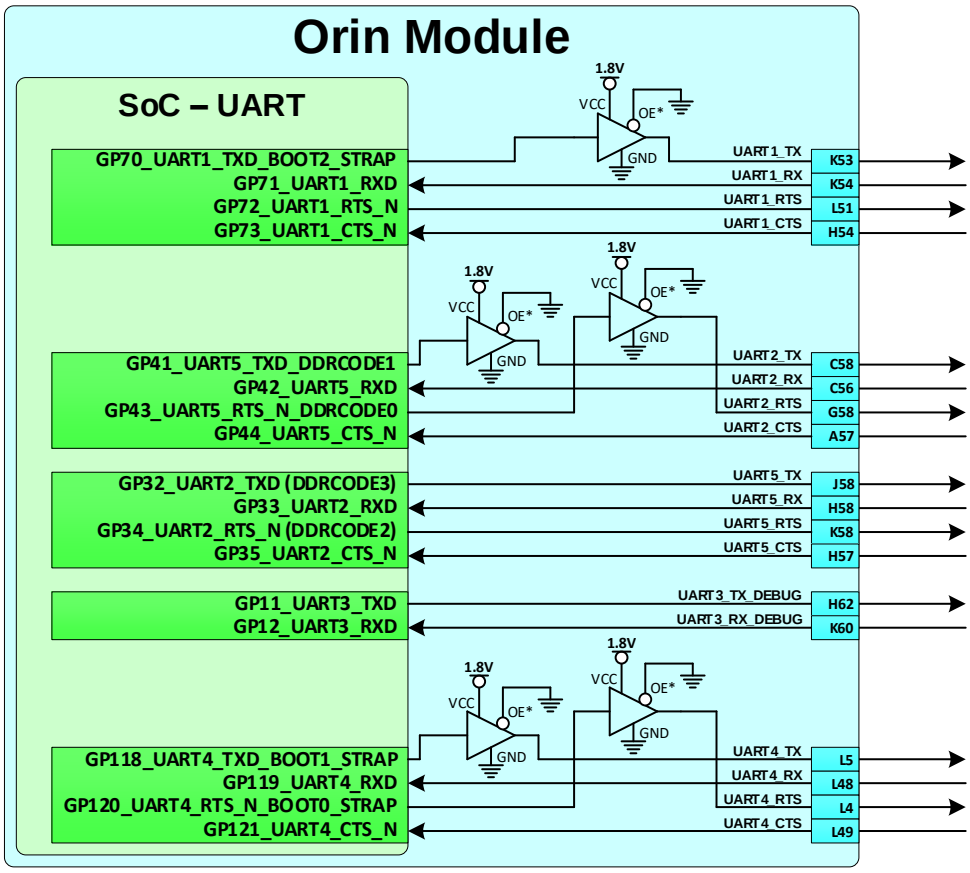
Table 15-1. Orin Module UART Pin Description

Pin #	Module Pin Name (SoC UART function)	SoC Signal	Usage/Description	Direction	Pin Type
K53	UART1_TX	GP70_UART1_TXD_BOOT2_STRAP	UART 1 Transmit	Output	CMOS – 1.8V
K54	UART1_RX	GP71_UART1_RXD	UART 1 Receive	Input	
L51	UART1_RTS	GP72_UART1_RTS_N	UART 1 Request to Send	Output	
H54	UART1_CTS	GP73_UART1_CTS_N	UART 1 Clear to Send	Input	
C58	UART2_TX	GP41_UART5_TXD_DDRCODE1	UART 2 Transmit	Output	CMOS – 1.8V
C56	UART2_RX	GP42_UART5_RXD	UART 2 Receive	Input	
G58	UART2_RTS	GP43_UART5_RTS_N_DDRCODE0	UART 2 Request to Send	Output	
A57	UART2_CTS	GP44_UART5_CTS_N	UART 2 Clear to Send	Input	
H62	UART3_TX_DEBUG	GP11_UART3_TXD	Debug UART Transmit	Output	CMOS – 1.8V
K60	UART3_RX_DEBUG	GP12_UART3_RXD	Debug UART Receive	Input	
L5	UART4_TX	GP118_UART4_TXD_BOOT1_STRAP	UART 4 Transmit	Output	CMOS – 1.8V
L48	UART4_RX	GP119_UART4_RXD	UART 4 Receive or I2S	Input	
L4	UART4_RTS	GP120_UART4_RTS_N_BOOT0_STRAP	UART 4 Request to Send	Output	
L49	UART4_CTS	GP121_UART4_CTS_N	UART 4 Clear to Send or I2S	Input	
J58	UART5_TX	GP32_UART2_TXD (DDRCODE2)	UART 5 Transmit	Output	CMOS – 1.8V
H58	UART5_RX	GP33_UART2_RXD	UART 5 Receive	Input	
K58	UART5_RTS	GP34_UART2_RTS_N (DDRCODE2)	UART 5 Request to Send	Output	
H57	UART5_CTS	GP35_UART2_CTS_N	UART 5 Clear to Send	Input	

Notes:

1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for bidirectional signals.
2. The direction indicated for the UART pins is true when used for that function. Otherwise, these pins support GPIO functionality and can support both input and output (bidirectional). The exception is the UART pins that are buffered on the module to shield most of the SoC strap related pins. This includes UART[4:2]_TX/RTS and UART1_TX. In addition, UART5_TX/RTS which are SoC strap pins should be included. These pins can only be used as outputs if selected as GPIOs.
3. Some functions are shared with other functions. Only one function can be used in a design. Ensure no conflicts exist when choosing the functions for a design.

Figure 15-1. Orin Module UART Connections



Note: UART pins that are used as SoC straps are buffered to keep connected devices from affecting the strap value when the system powers on.

Table 15-2. UART Signal Connections

Module Pin Name	Type	Termination	Description
UARTx_TX	O		UART Transmit: Connect to Peripheral RXD pin of device
UARTx_RX	I		UART Receive: Connect to Peripheral TXD pin of device
UARTx_CTS	I		UART Clear to Send: Connect to Peripheral RTS_N pin of device
UARTx_RTS	O		UART Request to Send: Connect to Peripheral CTS pin of device

15.1.1 UART Design Guidelines

Table 15-3 contains the signal routing requirements for the UART interface.

Table 15-3. UART Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate	4.25	Mbps	
Configuration / Device Organization	1	load	
Reference plane	GND		
Trace Impedance	40-60	Ω	±10%
Breakout	75	ps	
Via proximity (Signal via to GND return via)	< 3.8 (24)	mm (ps)	See note 1
Min Trace spacing Microstrip / Stripline	4x / 3x	Dielectric height	
Max Trace Length (Delay)	355 (2268)	mm (ps)	Assuming 6.3 ps/mm propagation delay.
Max Trace Delay Skew from RXD to TXD	38 (240)	mm (ps)	Assuming 6.3 ps/mm propagation delay.

Note: Up to four signal vias can share a single GND return via

Chapter 16. CAN

The Orin module brings two controlled area network (CAN) interfaces out to the main connector.

Table 16-1. Orin Module CAN Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
D59	CAN0_DOUT	GP17_CAN0_DOUT	CAN 0 Transmit	Output	CMOS – 3.3V
F58	CAN0_DIN	GP18_CAN0_DIN	CAN 0 Receive	Input	CMOS – 3.3V
H61	CAN1_DOUT	GP19_CAN1_DOUT	CAN 1 Transmit	Output	CMOS – 3.3V
B61	CAN1_DIN	GP20_CAN1_DIN	CAN 1 Receive	Input	CMOS – 3.3V

Notes:

1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. The direction indicated for CANx is associated with their use as CAN DOUT/DIN. The pins support GPIO functionality, so support both input and output operation (bidirectional).

Figure 16-1. Orin Module CAN Connections

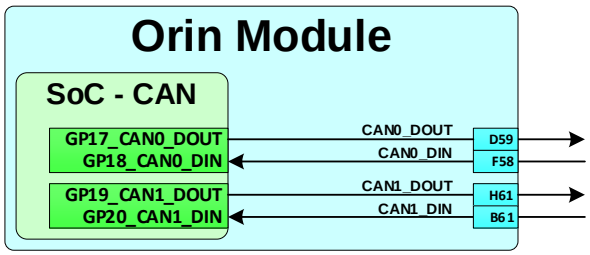


Table 16-2. CAN Signal Connections

Module Pin Name (Function)	Type	Termination	Description
CANx_DOUT	O		CAN Data Output: Connect to matching pin of device
CANx_DIN	I		CAN Input: Connect to Peripheral pin of device

16.1 CAN Design Guidelines

Table 16-3 contains the signal routing requirements for the CAN interface.

Table 16-3. CAN Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate / Frequency	8	Mbps / MHz	
Configuration / Device Organization	1	load	
Trace Impedance	45-50	Ω	±15%
Reference plane	GND or PWR		See note 1
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See note 2
Trace spacing - Microstrip / Stripline	3x / 2x	dielectric height	
PCB noise avoidance	3x	dielectric height	
Max PCB breakout length (delay)	6.5 (40)	mm (ps)	
Max Trace Length (delay)	307 (1933)	mm (ps)	
Max Trace Skew Length (Delay)	8 (50)	mm (ps)	

Note:

1. If PWR, add 2x 0201 0.1uF and 2x 0402 4.7uF decoupling capacitors between PWR and GND for return current.
2. Up to 4 signal vias can share a single GND return via.

Chapter 17. Fan

Orin module provides PWM and Tachometer functionality for controlling a fan as part of the thermal solution.

- The FAN_PWM pin is configured as GP_PWM3
- The FAN_TACH pin is configured as NV_THERM_FAN_TACH0

Table 17-1. Orin Module Fan Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type
E54	FAN_TACH	GP62	Fan Tachometer signal	Bidir	CMOS – 1.8V
K62	FAN_PWM	GP31_PWM3	Fan Pulse Width Modulation signal	Bidir	Open-Drain, 1.8V (3.3V tolerant, back-drive capable to 1.8V)

Notes:

1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. The direction indicated for FANx is associated with their use as Fan PWM/Tach. The pins support GPIO functionality, so support both input and output operation (bidirectional).

Figure 17-1. Orin Module Fan Connection Example

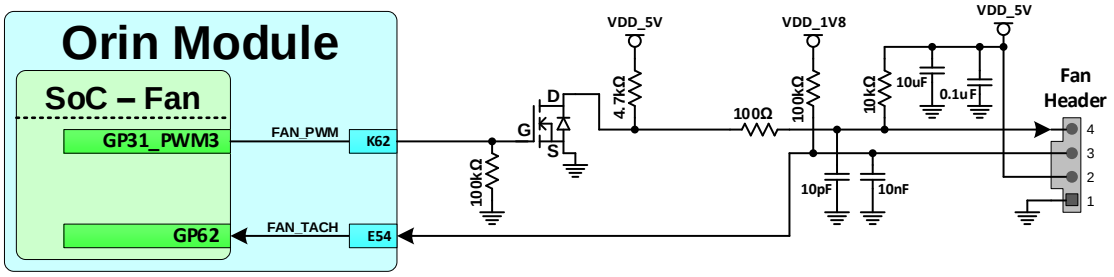


Table 17-2. Fan Signal Connections

Module Pin Name	Type	Termination	Description
FAN_PWM	O	100kΩ pulldown to GND, FET, . 10kohm pullup to VDD_5V and series 100Ω resistor.	Fan Pulse Width Modulation: Connect through FET as shown in the Orin module Fan Connections figure.
FAN_TACH	I	100kohm pullup to VDD_1V8	Fan Tachometer: Connect to TACH pin on fan connector.

Chapter 18. Debug

This chapter covers the interfaces that are provided for debug and development.

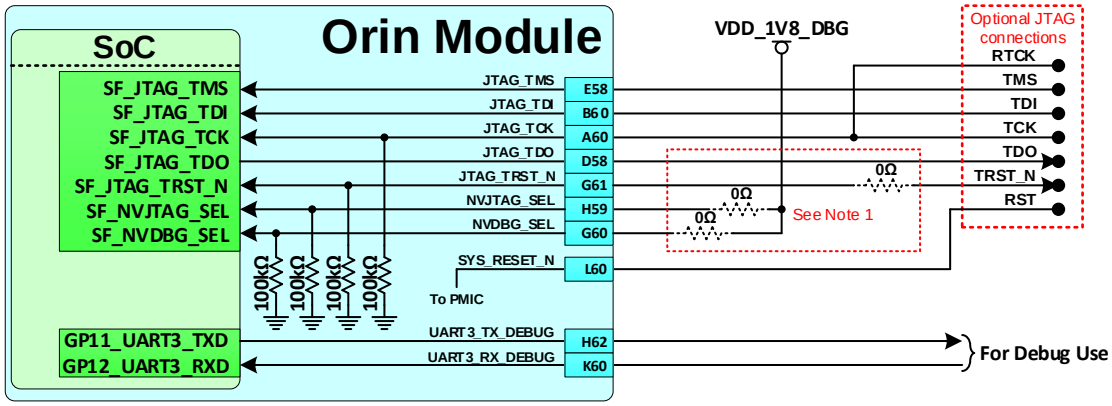
18.1 USB Recovery Mode

USB Recovery mode provides an alternate boot device (USB). In this mode, the system is connected to a host system and boots over USB. This is used when a new image needs to be flashed, or for debug purposes. To enter USB recovery mode, the FORCE_RECOVERY_N pin is held low when the system is powered on. FORCE_RECOVERY_N is the SoC RCM0 strap. Recovery mode can operate in either USB 2.0 or USB 2.0 + USB 3.2 modes. Recovery mode using USB 2.0 is from interface USB0_N/P only. No other signals are required or supported for entering Force Recovery mode. Neither VBUS nor ID detection is needed. If the force recovery strap is held low coming out of reset, Jetson AGX Orin will configure USB0 as a device and enter recovery mode. For USB 3.2 recovery mode, the USB 3.2 port must be Port #1 on the UPHY_RX1/TX1 pins.

18.2 JTAG and Debug UART

Figure 18-1 shows the JTAG and UART debug connections.

Figure 18-1. JTAG and UART Debug Connections

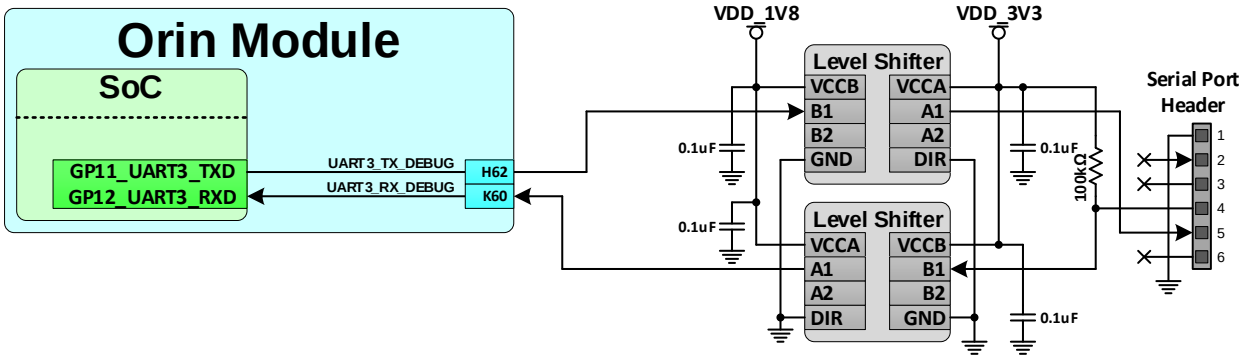


Notes:

1. NVJTAG_SEL and JTAG_TRST_N must be low for normal operation and pulled to 1.8V for Boundary Scan Mode. NVDBG is left unconnected (pulled down on module) for normal operation and pulled to 1.8V for alternate debug modes (debug over USB, etc.). for Boundary Scan test mode, JTAG_TRST_N must be driven high in the proper sequence. See the *Orin Module Boundary Scan Requirements and Usage* document for details.
2. Refer to preferred JTAG debugger documentation for JTAG PU/PD recommendations.

A simplified example to bring the debug UART out is shown in Figure 18-2. The UART3_DEBUG interface is shown routed to a 6-pin header through level shifters.

Figure 18-2. Simple Debug UART Header Connections



18.2.1 JTAG

JTAG is not required but may be useful for new design bring up or for boundary scan.

Table 18-1. Orin Module JTAG Pin Description

Pin #	Module Pin Name	SoC Signal	Usage/Description	Direction	Pin Type	MPIO Pad Code	Power-on Reset
H59	NVJTAG_SEL	SF_NVJTAG_SEL	NVIDIA JTAG Select. Low for normal operation or Arm JTAG debug mode. High for scan test mode. Pulled to GND through 100kΩ resistor on module.	Input Input	CMOS – 1.8V	JT_RST	z
G60	NVDBG_SEL	SF_NVDBG_SEL	NVIDIA Debug Select. Pulled to GND through 100kΩ resistor on module.		CMOS – 1.8V	JT_RST	z
A60	JTAG_TCK	SF_JTAG_TCK	JTAG Test Clock. Pulled to GND through 100kΩ resistor on module.	Input	CMOS – 1.8V	JT_RST	z
E58	JTAG_TMS	SF_JTAG_TMS	JTAG Test Mode Select	Input	CMOS – 1.8V	JT_RST	pu
D58	JTAG_TDO	SF_JTAG_TDO	JTAG Test Data Out	Output	CMOS – 1.8V	ST	z
B60	JTAG_TDI	SF_JTAG_TDI	JTAG Test Data In	Input	CMOS – 1.8V	JT_RST	pu
G61	JTAG_TRST_N	SF_JTAG_TRST_N	JTAG Test Reset. Low for normal operation or Arm JTAG debug mode. High for scan test mode. Pulled to GND through 100kΩ resistor on module.	Input	CMOS – 1.8V	JT_RST	pd

Notes:

1. In the Direction column, Output is from Orin module. Input is to Orin module. Bidir is for Bidirectional signals.
2. The MPIO Pad Codes are described in the *Orin (SoC) Technical Reference Manual* "Multi-Purpose I/O Pins and Pin Multiplexing (PinMux)" section for details.
3. The Power-on Reset State column indicates the pin state when reset is active and when it is deactivated before any changes are made by software. "z" is tristate, pu/pd indicates internal weak pull-up/down resistor is enabled, 1/0 indicates actively driven high/low.

Table 18-2. JTAG Signal Connections

Module Pin Name	Type	Termination	Description
JTAG_TMS	I		JTAG Mode Select: Connect to TMS pin of connector
JTAG_TCK	I	100kΩ to GND on module	JTAG Clock: Connect to TCK pin of connector
JTAG_TDO	O		JTAG Data Out: Connect to TDO pin of connector
JTAG_TDI	I		JTAG Data In: Connect to TDI pin of connector
JTAG_RTCK	I		JTAG Return Clock: Connect to RTCK pin of connector
JTAG_TRST_N	I	100kΩ to GND and 0.1uF to GND on module	JTAG General Purpose Pin #0: Leave unconnected for normal or Arm JTAG operation. Connect to TRST pin of connector or similar for Boundary Scan test mode. See the *Orin Module Boundary Scan Requirements and Usage* document for details.
NVJTAG_SEL		100kΩ to GND on module	NVIDIA JTAG Select: Used as select • Normal operation: Must be low, so leave unconnected (on-module pulldown will keep low). • Scan test mode: Connect NVJTAG_SEL to VDD_1V8. See Chapter 20: Boundary Scan Test Mode for details.
NVDBG_SEL		100kΩ to GND on module	NVIDIA Debug Select: Used as select • Normal operation: Leave series resistor from NVDBG_SEL not stuffed. • Advanced Debug modes: Connect NVDBG_SEL to VDD_1V8 (install 0Ω resistor as shown).

18.2.2 Debug UART

Orin module provides UART3_DEBUG for debug purposes. The connections are described in Table 18-3.

Table 18-3. Debug UART Connections

Module Pin Name	Type	Termination	Description
UART3_TX_DEBUG	O		UART Transmit: Connect to RX pin of serial device
UART3_RX_DEBUG	I	If level shifter implemented, 100 kΩ pull-up to supply on the non-Orin module side of the device.	UART Receive: Connect to TX pin of serial device

Chapter 19. Strapping Pins

Orin module has one strap (FORCE_RECOVERY_N) that is intended to be used on the carrier board. The FORCE_RECOVERY_N strap is used to enter Force Recovery mode by holding it low during power-on. Several other straps mentioned in this section are reserved for use on the module by NVIDIA only. Their state at power-on must not be affected by any connections on the carrier board.

The module includes buffers on all but two to ensure the SoC strapping pins retain their strapped state regardless of connections on the carrier board. For the unbuffered strap pins, the carrier board must ensure these pins are not pulled or driven low or high during power-on to avoid affecting the strap levels. Figure 19-1 shows an example of a buffer used to isolate the signals from any of the pins listed from the device they are connected to on the carrier board.

Figure 19-1. Example Buffer for SoC Strap Isolation

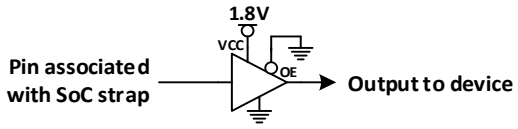
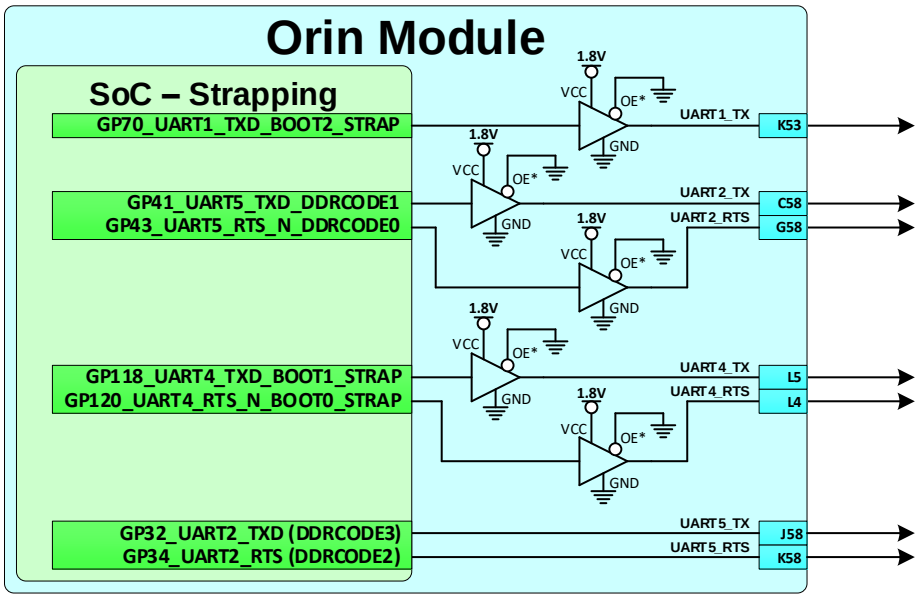


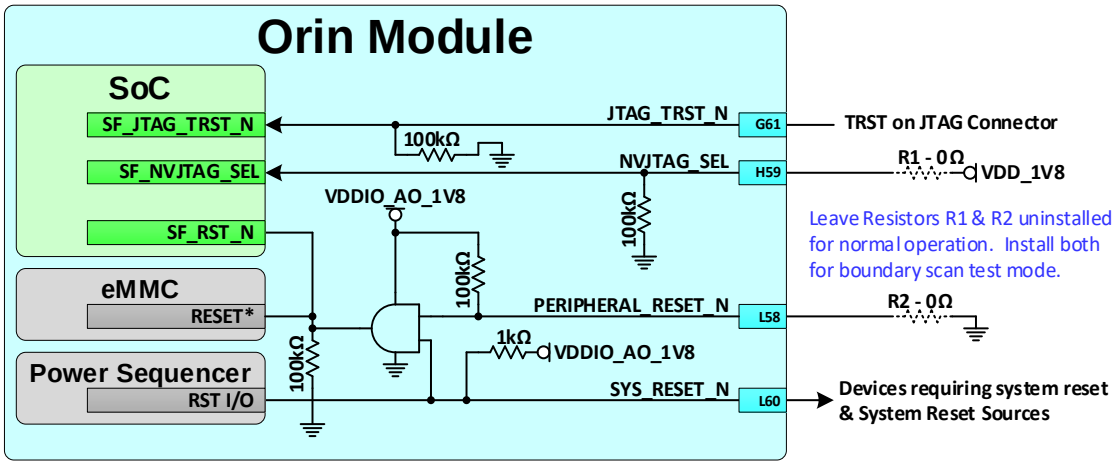
Figure 19-2. Orin Module Strap Pins



Chapter 20. Boundary Scan Test Mode

To enter the Boundary Scan Test mode, the NVJTAG_SEL pin must be pulled high and the SoC must be held in reset without resetting the Power Sequencer. This is achieved by using the PERIPHERAL_RESET_N pin on the module as illustrated in Figure 20-1.

Figure 20-1. Boundary Scan Connections



Chapter 21. Pads

21.1 MPIO Pad Behavior when Associated Power Rail is Enabled

Orin module CZ type MPIOs pins may glitch when the associated power rail is enabled or disabled. Designers should take this into account. MPIOs of this type that must maintain a low state even while the power rail is being ramped up or down may require special handling. The "Pin Descriptions" section of the Jetson AGX *Orin Data Sheet* includes the pin type information.

21.2 Schmitt Trigger Usage

The MPIO pins have an option to enable or disable Schmitt Trigger mode on a per-pin basis. This mode is recommended for pins used for edge-sensitive functions such as input clocks, or other functions where each edge detected will affect the operation of a device. Schmitt Trigger mode provides better noise immunity and can help avoid extra edges from being "seen" by the SoC inputs. Input clocks include the I2S and SPI clocks when SoC is in target mode. The FAN_TACH pin is another input that could be affected by noise on the signal edges. The SDCARD_CLK pin, while used to output the SD clock, also samples the clock at the input to help with read timing. Therefore, the pin may benefit from enabling Schmitt Trigger mode. Care should be taken if the Schmitt Trigger mode setting is changed from the default initialization mode as this can influence interface timing.

21.3 Pins Pulled and Driven During Power-on

Orin module is powered up before the carrier board (See Power Sequencing section). Some of the pins are pulled or driven high either by the SoC or by pull-up resistors on the module. The pins on Orin module that are pulled/driven high by the SoC can be found in the module pinmux spreadsheet. The pins that have pull-up resistors on the module are listed in the Orin module ¨Signal Terminations¨ section of the ¨Design Checklist¨ chapter. Care must be taken on the carrier board design to ensure that any of these pins that connect to devices on the carrier board (or devices connected to the carrier board) do not cause damage or excessive leakage to those devices. Some of the ways to avoid issues with sensitive devices are:

- External pull-downs on the carrier board that are strong enough to keep the signals low are one solution, given that this does not affect the function of the pin. This will not work pins actively driven high by default.
- Buffers or level shifters can be used to separate the signals from devices that may be affected. The buffer and shifter should be disabled until the device power is enabled.

Chapter 22. Unused Interface Terminations

22.1 Unused MPIO Interfaces

The following Orin module pins (and groups of pins) are Orin module MPIO (Multi-purpose Standard CMOS Pad) pins that support either special function IOs (SFIO) and/or GPIO capabilities. Any unused pins or portions of pin groups listed in Table 22-1 that are not used can be left unconnected.

Table 22-1. Unused MPIO Pins and Pin Groups

Module Pins / Pin Groups		Module Pins / Pin Groups		Module Pins and Pin Groups
I2Sx		PEX_Cx_CLKREQ_N/RST_N		SLEEP_REQ_N
CANx		PEX_WAKE_N		MODULE_SHDN_N
FANx		PWMx		THERM_ALERT_N
RGMIIx		SDCARDx		POWER_BTN_N
ENETx		SPIx		NVJTAG_SEL
GPIOx		SYSTEM_OC_N		NVDBG_SEL
DP2x		WDT_RESET_OUT_N		JTAGx
I2Cx		VCOMP_ALERT_N		UARTx
DPx_AUXx		MODULE_SLEEP_N		UFSx
MIDx		FORCE_RECOVERY_N		

22.2 Unused SFIO Interface Pins

Table 22-2 contains guidelines for unused dedicated special function I/O pins (SFIOs) for interfaces such as USB, PCIe, MGBE, HDMI, DisplayPort, and CSI.

Table 22-2. Unused SFIO Pin Terminations

Module Pin Name	Termination
USB 2.0	
USB[3:0]_N/P	Leave NC any unused pins
USB 3.2, PCIe, MGBE	
UPHY_TXx_N/P	Leave NC any unused TX lines
UPHY_RXx_N/P	Leave NC any unused RX lines or pull to GND through 10kohm resistors
UPHY_REFCLKx_N/P	Reference clock inputs: Leave NC or pull to GND through 10kohm resistors
PEX_CLKx_N/P	Reference clock outputs: Leave NC if not used
HDMI/DP	
HDMI_DP2_TX[3:0]_N/P	Leave NC any unused lanes
CSI	
CSI[7:0]_x_N/P	Leave NC any unused CSI lanes

Chapter 23. General Layout Guidelines

Trace and via characteristics play an important role in signal integrity and power distribution on Orin module. Vias can have a strong impact on power distribution and signal noise, so careful planning must take place to ensure designs meet the NVIDIA via requirements. Trace length or delay and impedance determine signal propagation time and reflections, both of which can greatly improve or reduce the performance of Orin module. Trace and via requirements for each signal type can be found in the corresponding chapter. This chapter provides general guidelines for via and trace placement.

23.1 Via Guidelines

The number of vias in the path of a given signal, power supply line, or ground line can greatly affect the performance of the trace. Via placement can make differences in current carrying capability, signal integrity (due to reflections and attenuation), and noise generation, all of which can impact the overall performance of the trace. The following guidelines provide basic advice for proper use of vias.

23.1.1 Via Count and Trace Width

As a rule, each ampere of current requires at least two micro-vias. A typical thru-hole via can handle two amperes of current.

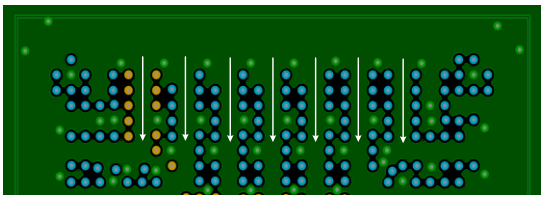
23.1.2 Via Placement

If vias are not placed carefully, they can severely degrade the robustness of a board's power plane. In standard designs that do not use blind or buried vias, construction of a via entails drilling a hole that cuts into the power and ground planes. Thus, incorrect via placement affects the amount of copper available to carry current to the power balls of the IC.

23.1.3 Via Placement and Power and Ground Corridors

Vias should be placed so that sufficiently wide power corridors are created for good power distribution, as show in Figure 23-1.

Figure 23-1. Via Placement for Good Power Distribution



Care should also be taken to avoid use of "thermal spokes" (also referred to as "thermal relief") on power and ground vias. Thermal spokes are not necessary for surface-mount components, and the narrow spoke widths contribute to increased inductance. The metal on the inner layers between vias may not be flooded with copper if enough spacing is not provided. The diminished spacing creates a blockage and forces the current to find another path due to lack of copper, as shown in Figure 23-2 and Figure 23-3. This leads to power delivery issues and impedance discontinuities when traces are routed over these plane voids.

Figure 23-2. Good Current Flow Resulting from Correct Via Placement

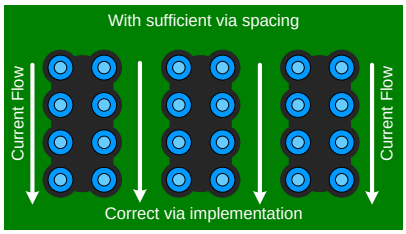
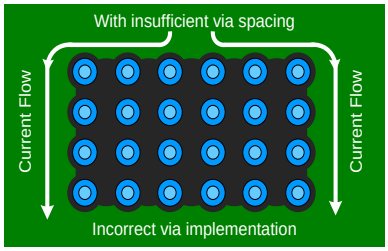


Figure 23-3. Poor Current Flow Resulting from Incorrect Via Placement



In general, a dense via population should be avoided and good PCB design principles and analysis should be applied.

23.2 Connecting Vias

To be effective, vias must be connected properly to the signal and power planes. Poor via connections make the capacitor and power planes less effective, leading to increased cost due to the need for additional capacitors to achieve equivalent performance. This not only impacts the Bill of Materials (BOM) cost of the design, but it can greatly impact quality and reliability of the design.

23.3 Trace Guidelines

Trace length/delay and impedance play a critical role in signal integrity between the driver and the receiver on Orin module. Signal trace requirements are determined by the driver characteristics, source characteristics, and signal frequency of the propagating signal.

23.3.1 Layer Stack-Up

The number of layers required is determined by the number of signal layers needed to achieve the desired performance, and the number of power rails required to achieve the optimum power delivery or noise floor. For example, high-performance boards require four signal routing layers, with at least two GND planes for reference. This comes to six layers; add another two for power, which gives eight layers minimum. Reduction from eight to six layers starts the trade-off of cost versus performance.

Power and GND planes usually serve two purposes in PCB design: power distribution and providing a signal reference for high-speed signals.

Either the power or the ground planes can be used for high-speed signal reference; this is particularly common for low-cost designs with a low layer count. When both power and GND are used for signal reference, make sure you minimize the reference plane transition for all high-speed signals. Decoupling caps or transition vias should be added close to the reference plane transitions.

23.3.2 Trace Length or Delay

The maximum trace length or delay for a given signal is determined by the maximum allowable propagation delay and impedance for the signal. Higher frequency signals must be treated as transmission lines (see Chapter 26 “Transmission Line Primer”) to determine proper trace characteristics for a signal.

All signals on the design maintain different trace guidelines. Refer to the corresponding signal chapter in the design guide to determine the guidelines for the signal.

Chapter 24. Stack-Ups

24.1 Reference Design Stack-ups

This section details the reference design stack-ups.

24.1.1 Importance of Stack-up Definition

Stack-ups define the number and order of board layers. Stack-up definition is critical to the following design:

- Circuit routability
- Signal quality
- Cost

24.1.2 Impact of Stack-up Definition on Design

- Stack-Up Impact on Circuit Routability
  If there are insufficient layers to maintain proper signal spacing, prevent discontinuities in reference planes, obstruct flow of sufficient current, or avoid extra vias, circuit routing can become unnecessarily complex. Layer count must be minimally appropriate for the circuit.
- Stack-Up Impact on Signal Quality
  Both layer count and layer order impact signal integrity. Proper inter-signal spacing must be achievable. Via count for critical signals must be minimized. Current commensurate with the performance of the board must be carried. Critical signals must be adjacent to major and minor reference planes and adhere to proximity constraints with respect to those planes. The recommended NVIDIA stack-ups achieve these requirements for the signal speeds supported by the board.
- Stack-Up Impact on Cost
  While defining extra layers can facilitate excellent signal integrity, current handling capability and routability, extra layers can impede the goal of hitting cost targets. The art of stack-up definition is achieving all technical and reliability circuit requirements in a cost-efficient manner. The recommended NVIDIA stack-ups achieve these requirements with efficient use of board layers.

Chapter 25. USB 3.2 and Wireless Coexistence

USB 3.2 supports a 5 Gbps (or multiple) signaling rate. The USB 3.2 specification requires USB 3.2 data to be scrambled and spread-spectrum is required. The noise from the USB 3.2 data spectrum has been found from around DC to 4 GHz and beyond. This noise can desensitize nearby receivers operating in the cellular and WiFi 2.4 GHz band. This includes, for example, WiFi 802.11b/g/n or Bluetooth® including Bluetooth mouse devices, Bluetooth keyboards, and so on. This noise causes:

- WiFi sensitivity degradation
- Wireless link throughput drop
- Wireless operation range degradation

This section is focusing on USB 3.2, but other high-speed interfaces such as HDMI, DP, and so on, can also cause issues with wireless subsystems. The issues and recommended mitigation techniques would be similar.

25.1 Mitigation Techniques

Each design is different due to unique construction and relative location of USB 3.2 circuits and connectors and receiving antenna. Depending on the level of noise generated, emitted, radiated, and coupled to receiver antenna, some or all of the recommendations might need to be implemented to limit unwanted noise from radiating from the circuit.

The following mitigation techniques described will help minimize the USB 3.2 de-sense.

INCREASE THE USB 3.2 TO ANTENNA SEPARATION

During the placement phase of the design, care must be taken to identify the noise source and try to physically increase the separation between the noise source and antenna. One of the major noise sources is the USB 3.2 connector itself. If possible, the antenna or USB 3.2 location can be changed to increase physical isolation. In general, doubling the distance between antenna and noise source, reduces the coupling by around 6 dB.

USB 3.2 CONNECTOR PART SELECTION: CHOOSE A BETTER USB 3.2 PART

A USB 3.2 connector has many metal fingers that are perfect in length for radiating in and around the 2.4 GHz band and beyond. A USB 3.2 connector should be selected to minimize radiation from the USB 3.2 part itself. Some recommendations are:

- Connector fully enclosed by metal
- No slots in the connector walls, or if there are slots, the size is very small. Also, the number of slots should be minimal.
- Connector has as many grounding legs as possible. More legs provide better grounding from the USB 3.2 exterior to the PCB and the structure is less likely to radiate. Choose four legged connectors over two legged connectors and so on.

The quality of the external USB 3.2 device used in the USB 3.2 port will have impact on the overall experience. If the external USB 3.2 device used in the USB 3.2 port is of poor quality, the part itself will radiate and issues will continue. A plastic base USB 3.2 device works inferior compared to fully metalized USB 3.2 devices.

GROUND THE USB 3.2 PART SOLIDLY

The USB 3.2 connector is grounded through "the grounding legs" previously mentioned. Care must be taken to ensure the leg area is a very good RF ground. One way to do this is to increase the number of ground vias placed in the "grounding leg" area.

IMPROVE THE ROUTING AND GROUNDING AROUND THE USB 3.2 PART AREA

The routing and grounding around the USB 3.2 connector part area must be handled carefully. Since this area is very "hot," any traces running on the surface layer below the physical connector part can pick up noise and transfer it to other areas or radiate the noise. These traces need to be moved to an inner layer, and this area needs to be made a very good ground.

BURY THE USB 3.2 LINES IN INNER LAYERS

The USB 3.2 lines should be routed as impedance controlled differential pairs, with ground on either side and on the layers above and below.

SHIELD THE USB 3.2 CONNECTOR PART

The radiation from the USB 3.2 connector part is very strong. Need to make a "shield" and put on top of the USB 3.2 connectors. The shield must touch the USB 3.2 body in multiple points. The shield track must have number of grounding vias so that any emitted noise from the USB 3.2 connector is swiftly grounded.

Chapter 26. Transmission Line Primer

26.1 Basic Board Level Transmission Line Theory

NVIDIA maintains strict guidelines for high-frequency PCB transmission lines to ensure optimal signal integrity for data transmission. This section provides a brief primer into basic board-level transmission line theory.

26.1.1 Characteristics

The most important PCB transmission line characteristics are listed in the following bullets:

- Trace width/height, PCB height and dielectric constant, and layer stack-up affect the characteristic trace impedance of a transmission line.

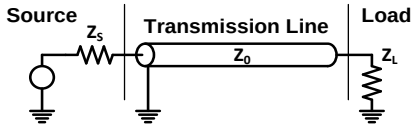
$$Z_0 \cong \left(\frac{L}{C}\right)^{1/2}$$

- Signal rise time is proportional to the transmission line impedance and load capacitance.

$$RiseTime \cong \left(\frac{Z_0 * R_{Term}}{Z_0 + R_{Term}}\right) * C_{Load}$$

- Real transmission lines (Figure 26-1) have non-zero resistances that lead to attenuation and distortion, creating signal integrity issues.

Figure 26-1. Typical Transmission Line Circuit



Transmission lines are used to "transmit" the source signal to the load or destination with as little signal degradation or reflection as possible. For this reason, it is important to design the high-speed signal transmission line to fall within characteristic guidelines based on the signal speed and type.

26.2 Physical Transmission Line Types

The two primary transmission line types often used for Orin module board designs are:

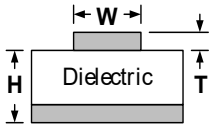
- Microstrip transmission line (Figure 26-2)
- Stripline transmission line (Figure 26-3)

The following sections describe each type of transmission.

26.2.1 Microstrip Transmission Line

Figure 26-2 describes the microstrip transmission line.

Figure 26-2. Microstrip Transmission Line



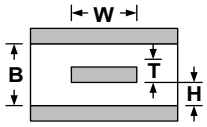
$$Z_0 = \left(\frac{87}{\sqrt{Er + 1.414}}\right) \ln\left(\frac{5.98H}{0.8W + T}\right)$$

- Z0: Impedance
- W: Trace width
- T: Trace thickness
- Er: Dielectric constant of substrate
- H: Distance between signal and reference plane

26.2.2 Stripline Transmission Line

Figure 26-3 describes the microstrip transmission line.

Figure 26-3. Stripline Transmission Line



$$Z_0 = \left(\frac{60}{\sqrt{Er}}\right) \ln\left(\frac{4H}{0.67\pi W\left(0.8 + \frac{T}{W}\right)}\right)$$

- Z0: Impedance
- W: Trace width (inches)
- T: Trace thickness (inches)
- Er: Dielectric constant of substrate
- H: Distance between signal and reference plane

26.3 Drive Characteristics

Driver characteristics are important to the integrity and maximum speed of the signal. The following points identify key driver equations and concepts used to improve signal integrity and transmission speed.

- The driver (source) has resistive output impedance Z_S, which causes only a fraction of the signal voltage to propagate down the transmission line to the receiver (load).
  - Transfer function at source:

$$T1 = \frac{Z_0}{Z_S + Z_0}$$

  - Driver strength is inversely proportional to the source impedance, Z_S.
- Z_S also acts as the source termination, which helps dampen reflection.
  - Source reflection coefficient:

$$R1 = \frac{(Z_S - Z_0)}{(Z_S + Z_0)}$$

26.4 Receiver Characteristics

Receiver characteristics are important to the integrity and detectability of the signal. The following points identify key receiver concepts and equations for optimum signal integrity at the final destination.

- The receiver acts as a capacitive load and often has a high load impedance, Z_L.
- Unterminated transmission lines cause overshoot and reflection at the receiver, which can cause data corruption.
  - Output transfer function at load:

$$T2 = \frac{2 * Z_L}{Z_L + Z_0}$$

  - Load reflection coefficient:

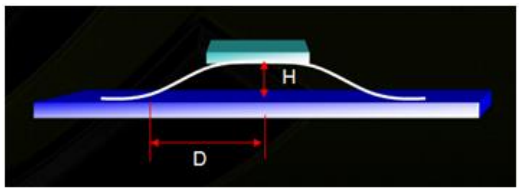
$$R2 = \frac{(Z_L - Z_0)}{(Z_L + Z_0)}$$

- Load impedance can be lowered with a termination resistor (R_{Term}) placed at the end of the transmission line.
  - Reflection is minimized when Z_L matches Z_0

26.5 Transmission Lines and Reference Planes

Defining an appropriate reference plane is vital to transmission line performance due to crosstalk and EMI issues. The following points explore appropriate reference plane identification and characteristics for optimal signal integrity:

Figure 26-4. Transmission Line Height



- Transmission line return current:
  - High-speed return current follows the path of least inductance.
  - The lowest inductance path for a transmission line is the portion of the line closest to the dielectric surface; i(D) is proportional to

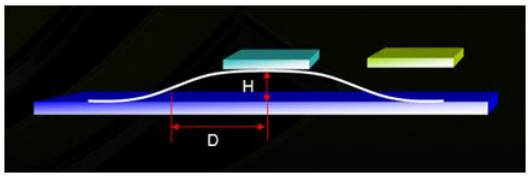
$$\frac{1}{\left(1+\left(\frac{D}{H}\right)^2\right)}$$

- Crosstalk on solid reference plane (Figure 26-5):
  - Crosstalk is caused by the mutual inductance of two parallel traces.
  - Crosstalk at the second trace is proportional to

$$\frac{1}{\left(1+\left(\frac{D}{H}\right)^2\right)}$$

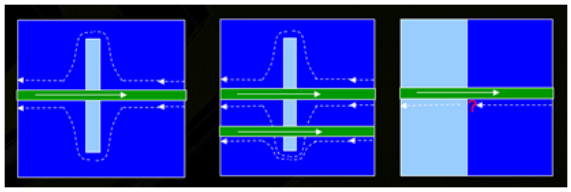
  - The signals need to be properly spaced to minimize crosstalk

Figure 26-5. Crosstalk on Reference Plane



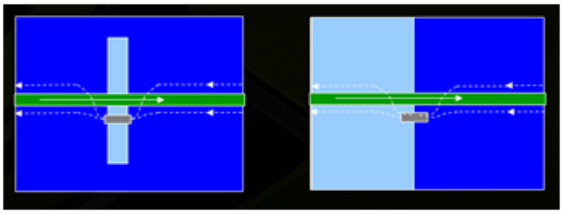
- Reference plane selection
  - Solid ground is preferred as reference plane.
  - Solid power can be used as reference plane with decoupling capacitors near driver and receiver.
  - Reference plane cuts and layer changes need to be avoided.
- Power plane cut example (Figure 26-6)
  - Power plane cuts will cause EMI issues.
  - Power plane cuts also induce crosstalk to adjacent signals.

Figure 26-6. Power Plane Cuts Example



- When a cut is unavoidable:
  - Place decoupling capacitors near transition.
  - Place transition near source or receiver when decoupling capacitors are abundant (Figure 26-7).

Figure 26-7. Power Plane Cuts Example when Decouple Capacitors are abundant



- When signal changes plane:
  - Try not to change the reference plane, if possible.
  - When a reference plane switches to different power rail, a stitching capacitor is required (Figure 26-8).
  - When the same ground and power reference plane changes to a different layer, a stitching via is required (Figure 26-9).

Figure 26-8. Switching Reference Planes

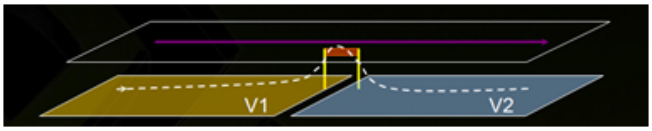
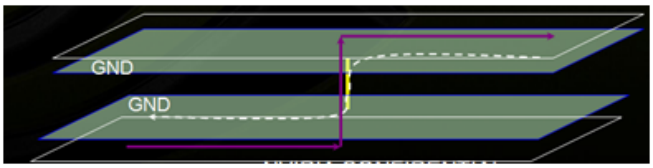


Figure 26-9. Reference Plane Switch Using Via



Chapter 27. Design Guideline Glossary

The design guidelines include various terms. The following descriptions are intended to show what these terms mean and how they should be applied to a design.

- Trace Delay
  - Max Breakout Delay
    Routing on Component layer: Maximum Trace Delay from module connector pin to point beyond pin array where normal trace spacing/impedance can be met. Routing passes to layer other than Component layer: Beyond this, normal trace spacing/impedance must be met.
  - Max Total Trace Delay
    Trace from module connector pin to device pin. This must include routing on the main PCB and any other Flex or secondary PCB. Delay is from the module connector to the final connector and device.
- Intra and Inter Pair Skews
  - Intra Pair Skew within Pair
    Difference in delay between two traces in differential pair: Shorter routes may require indirect path to equalize delays.
  - Inter Pair Skew Pair-to-Pair
    Difference between two (or possibly more) differential pairs.
- Impedance and Spacing
  - Microstrip vs. Stripline
    - Microstrip: Traces next to single reference plane.
    - Stripline: Traces between two reference planes.
  - Trace Impedance
    Impedance of trace determined by width and height of trace, distance from reference plane, and dielectric constant of PCB material. For differential traces, space between pair of traces is also a factor.
  - Board Trace Spacing and Spacing to other Nets
    Minimum distance between two traces. Usually specified in terms of dielectric height which is distance from trace to reference layers.
  - Pair to Pair Spacing
    Spacing between differential traces.

- Breakout Spacing
  Possible exception to board trace spacing where different spacing rules are allowed under module connector pin to escape from the pin array. Outside device boundary, normal spacing rules apply.

- Reference Return
  - Ground Reference Return Via and Via proximity (signal to reference)
    - Signals changing layers and reference GND planes need similar return current path.
    - Accomplished by adding via, tying both GND layers together.
  - Via proximity (signal to reference) is distance between signal and reference return vias.
    - GND reference via for Differential Pair.
    - Where a differential pair changes GND reference layers, return via should be placed close to and between signal vias (example to right).
  - Signal to return via ratio
    Number of Ground Return vias per Signal vias. For critical IFs, ratio is usually 1:1. For less critical IFs, several trace vias can share fewer return vias (that is 3:2 – 3 trace vias and 2 return vias).
  - Slots in Ground Reference Layer
    - When traces cross slots in adjacent power or ground plane.
    - Return current has longer path around slot.
    - Longer slots result in larger loop areas.
    - Avoid slots in GND planes or do not route across them.
  - Routing over Split Power Layer Reference Layers
    - When traces cross different power areas on power plane.
      - Return current must find longer path - usually a distant bypass cap.
      - If possible, route traces with solid plane (GND or PWR) or keep routes across single area.
    - If traces must cross two or more power areas, use stitching capacitors.
      - Placing one cap across two PWR areas close to where traces cross area boundaries provide high-frequency path for return current.
      - Cap value typically 0.1uF and should ideally be within 0.1" of crossing.

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